

FIG. 1B

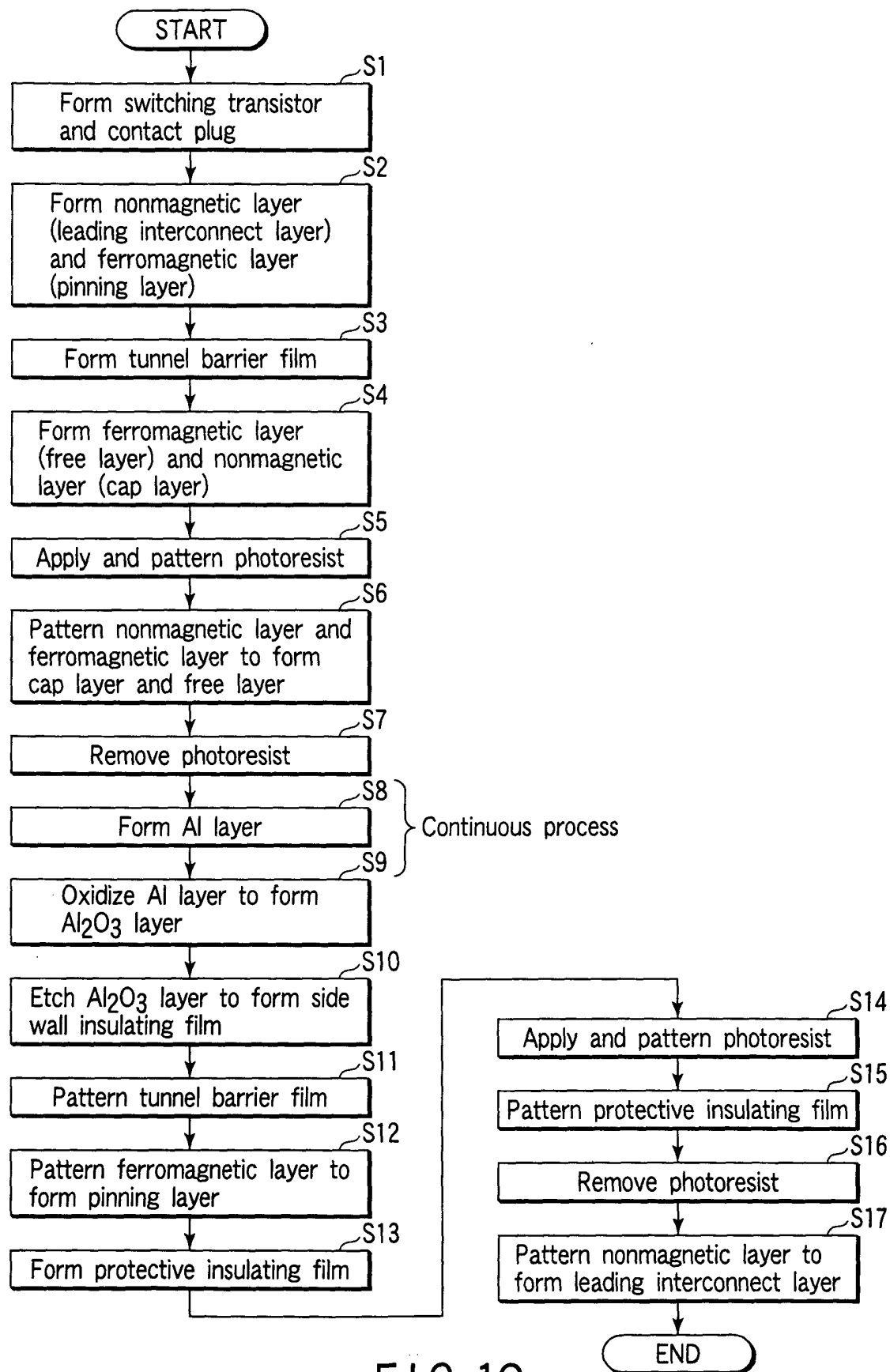


FIG. 1C

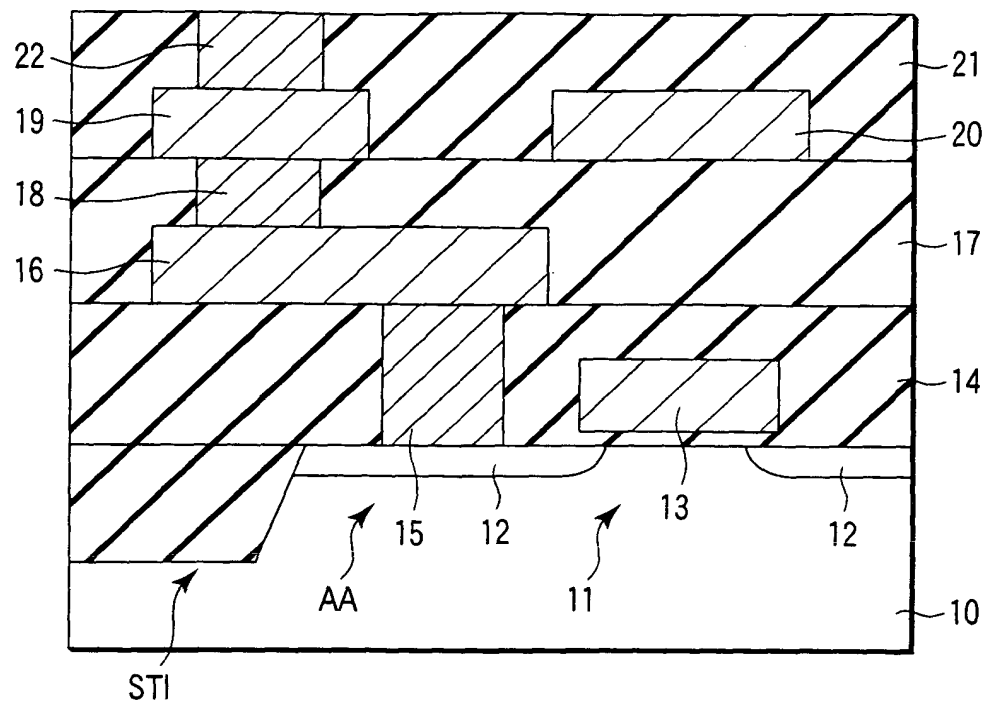


FIG. 2A

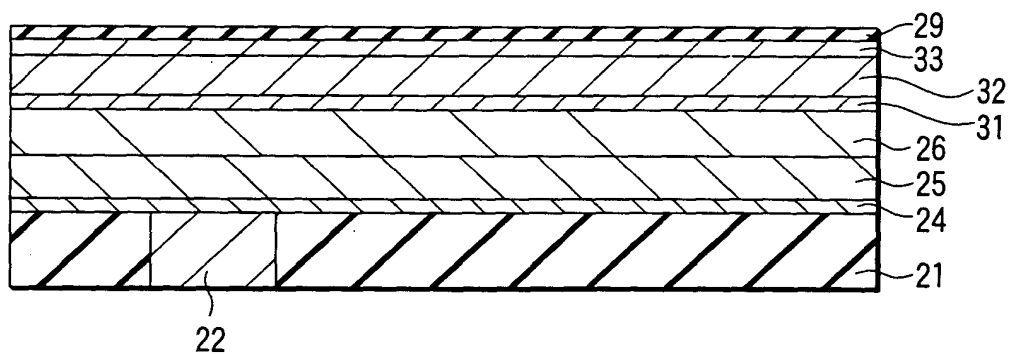


FIG. 2B

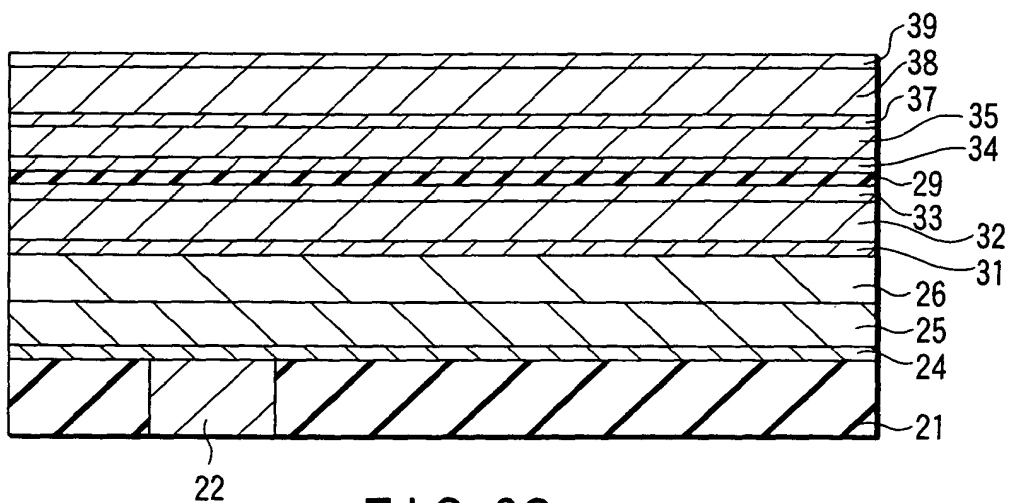


FIG. 2C

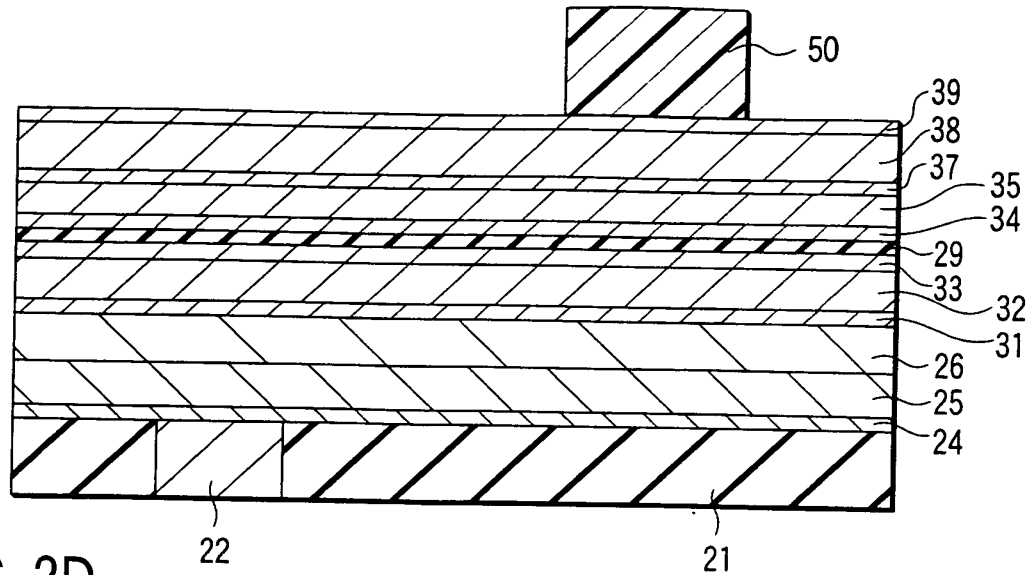


FIG. 2D

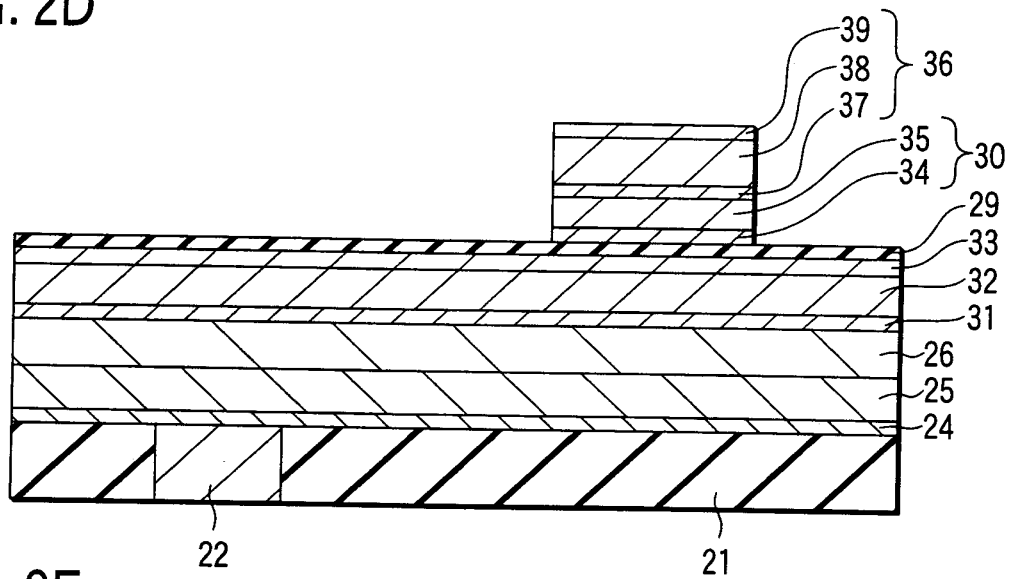


FIG. 2E

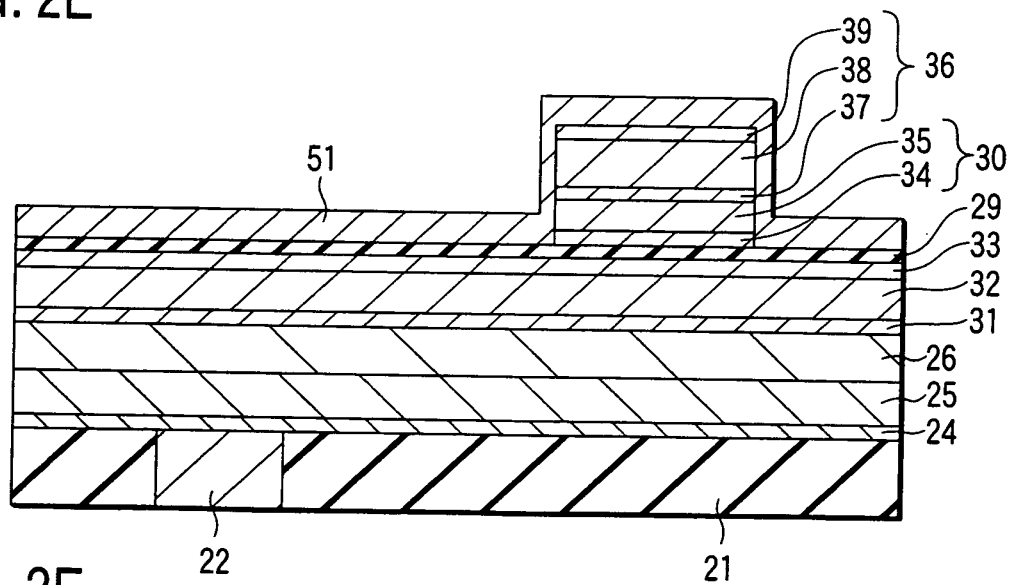


FIG. 2F

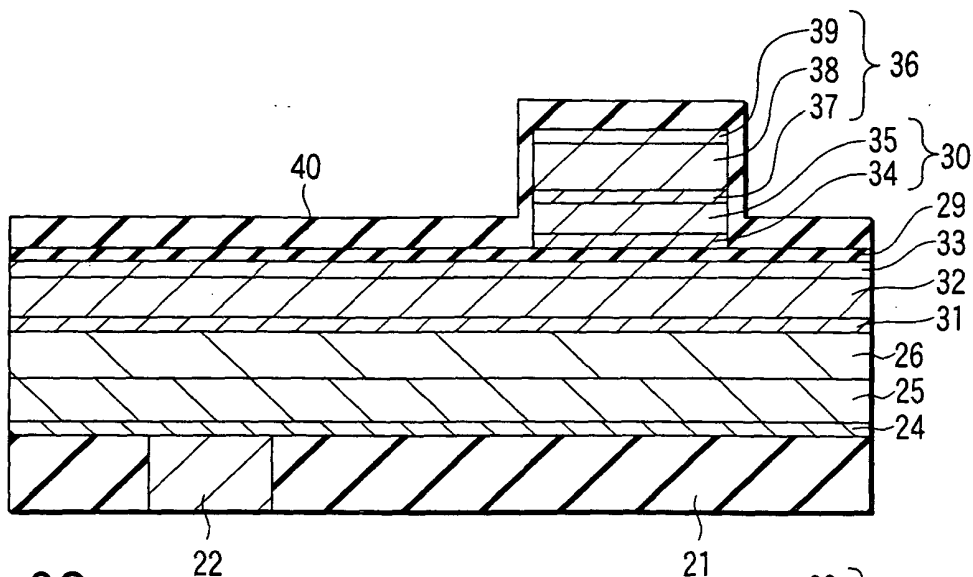


FIG. 2G

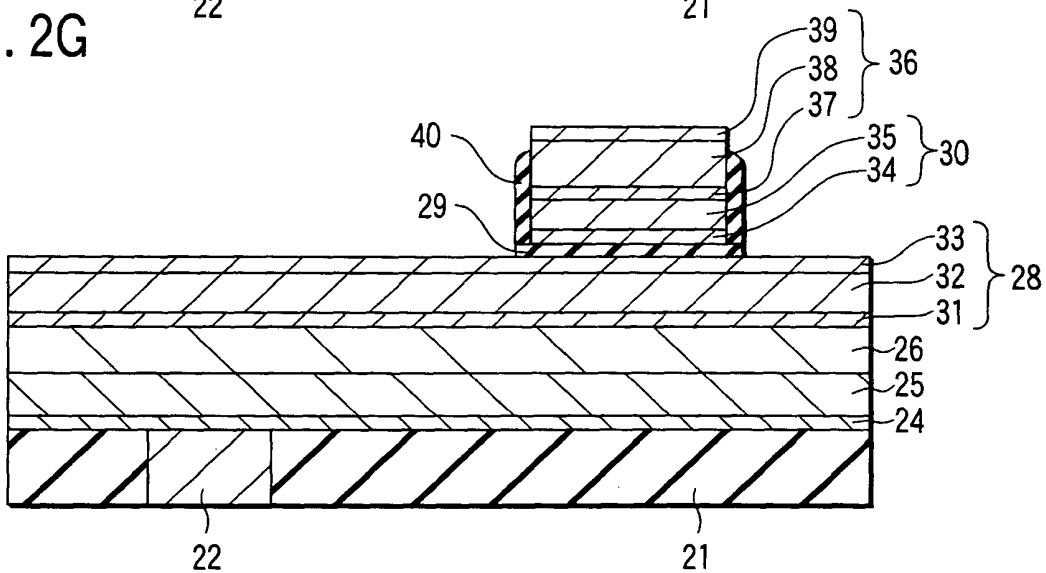


FIG. 2H

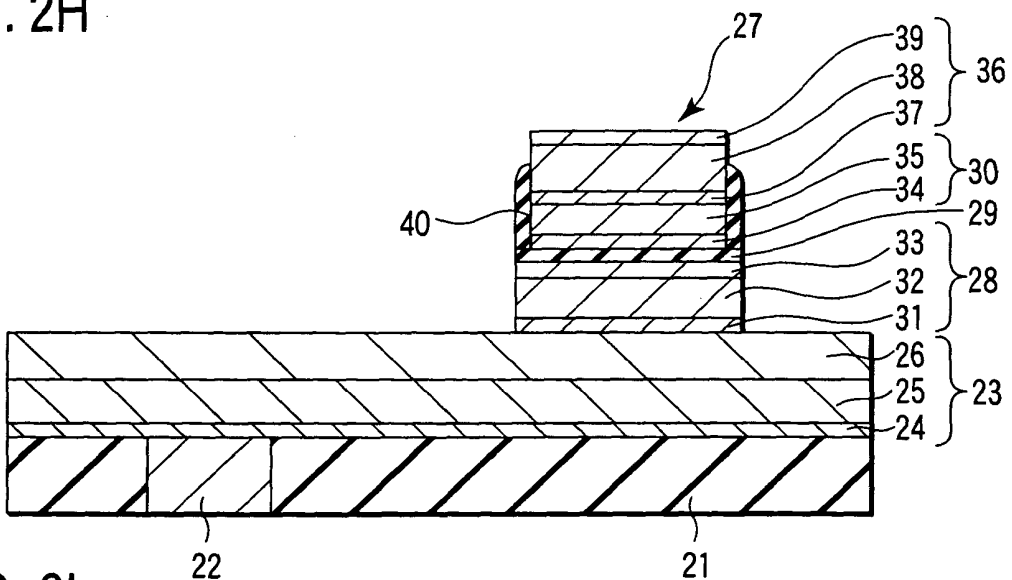


FIG. 2I

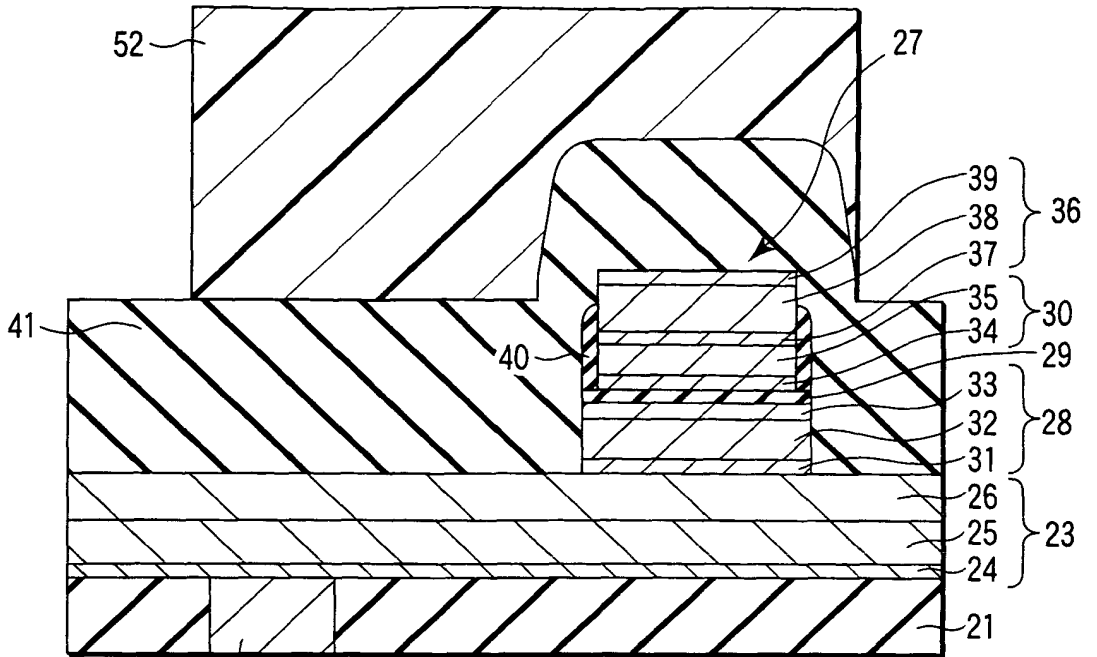


FIG. 2J

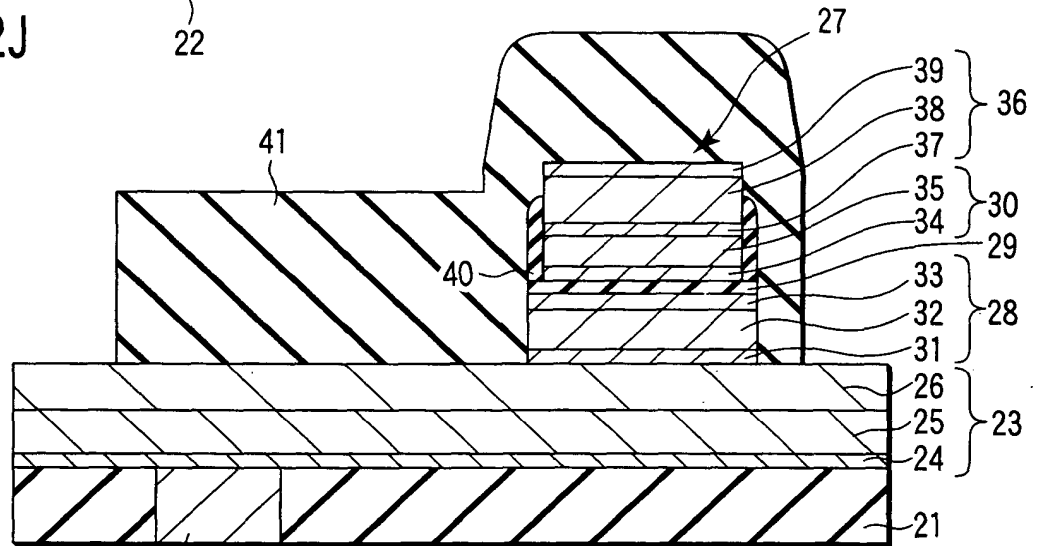


FIG. 2K

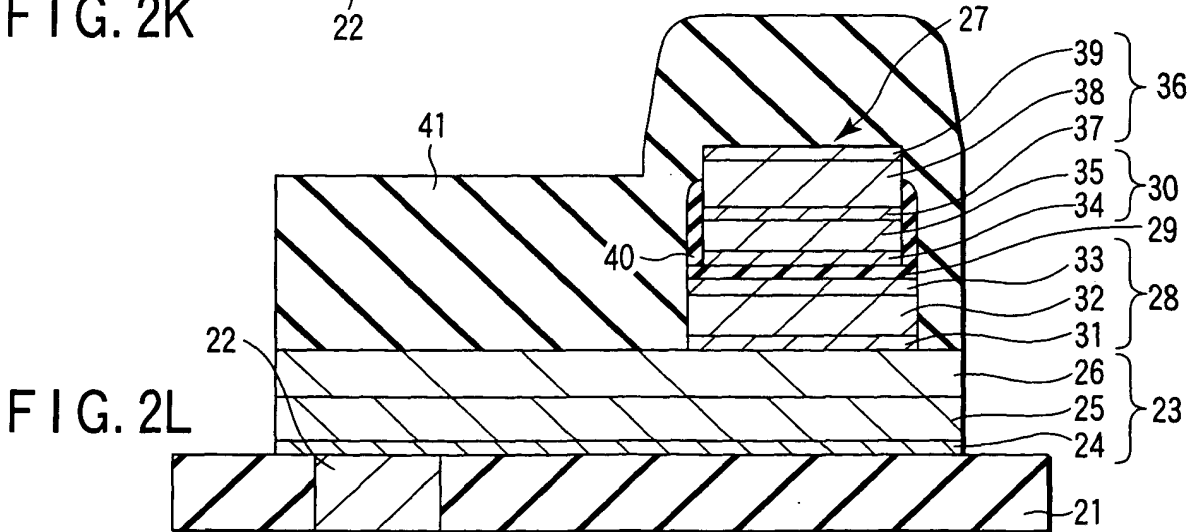


FIG. 2L

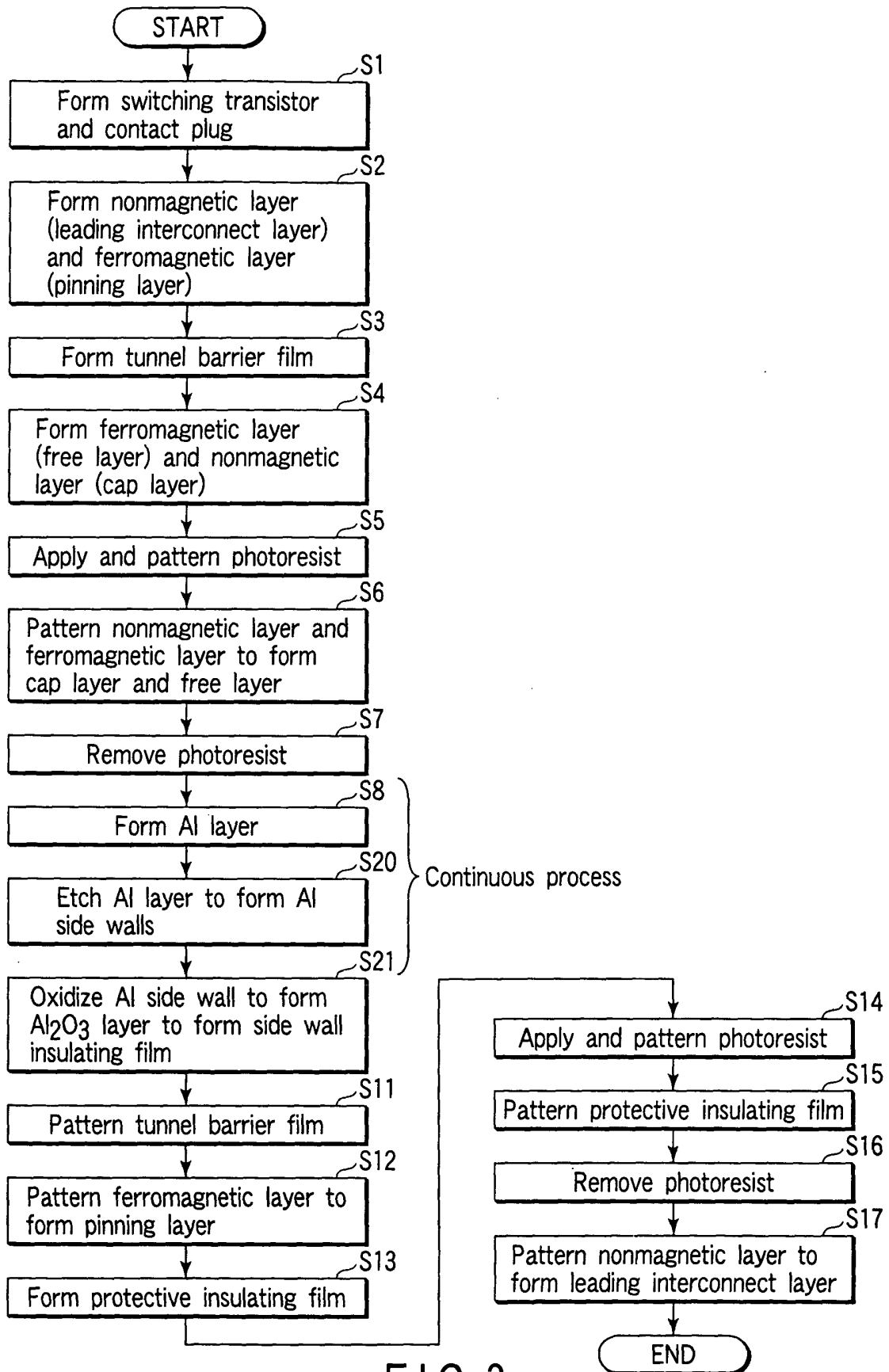


FIG. 3

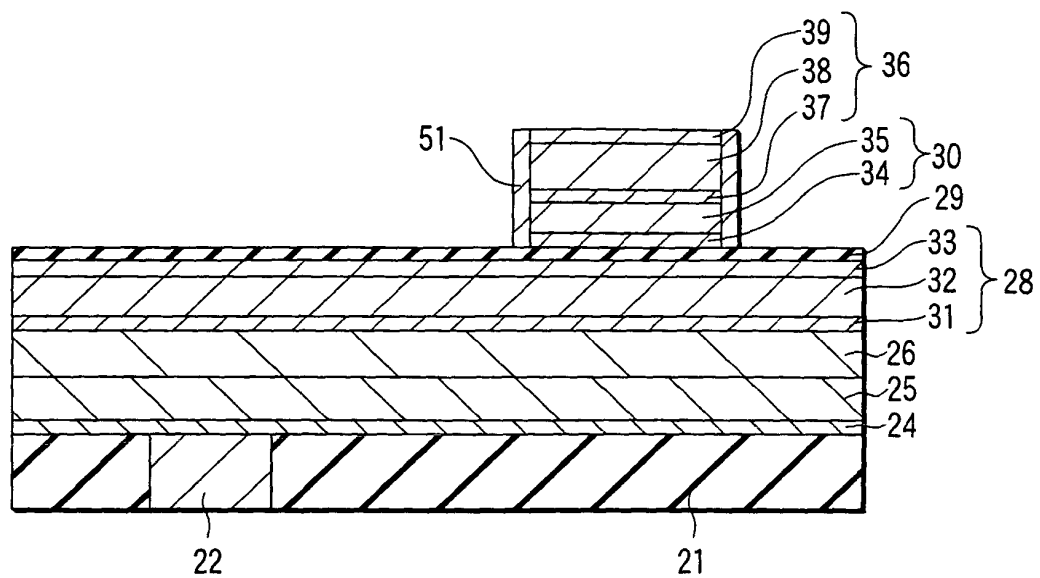


FIG. 4A

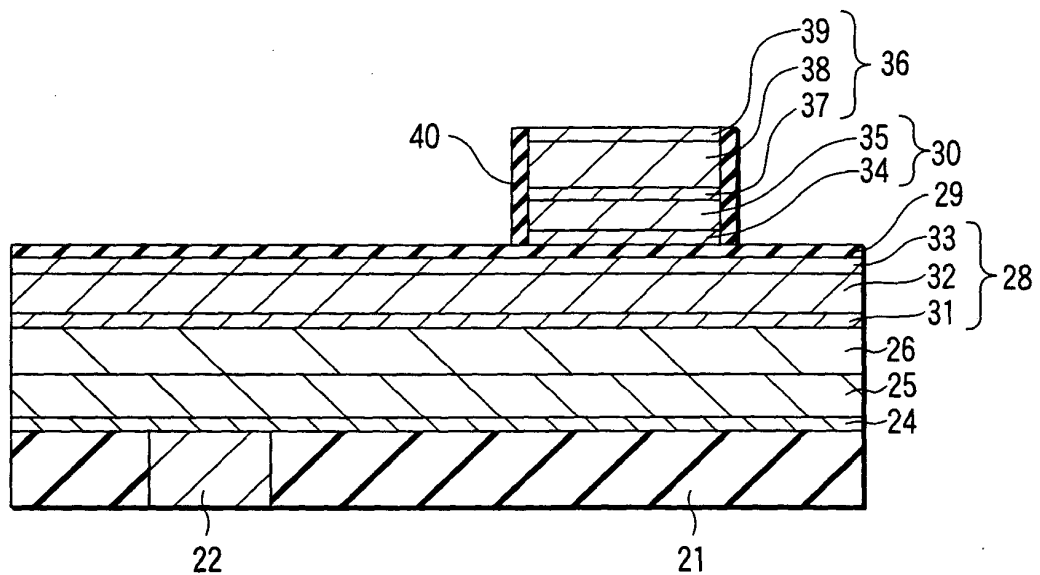


FIG. 4B

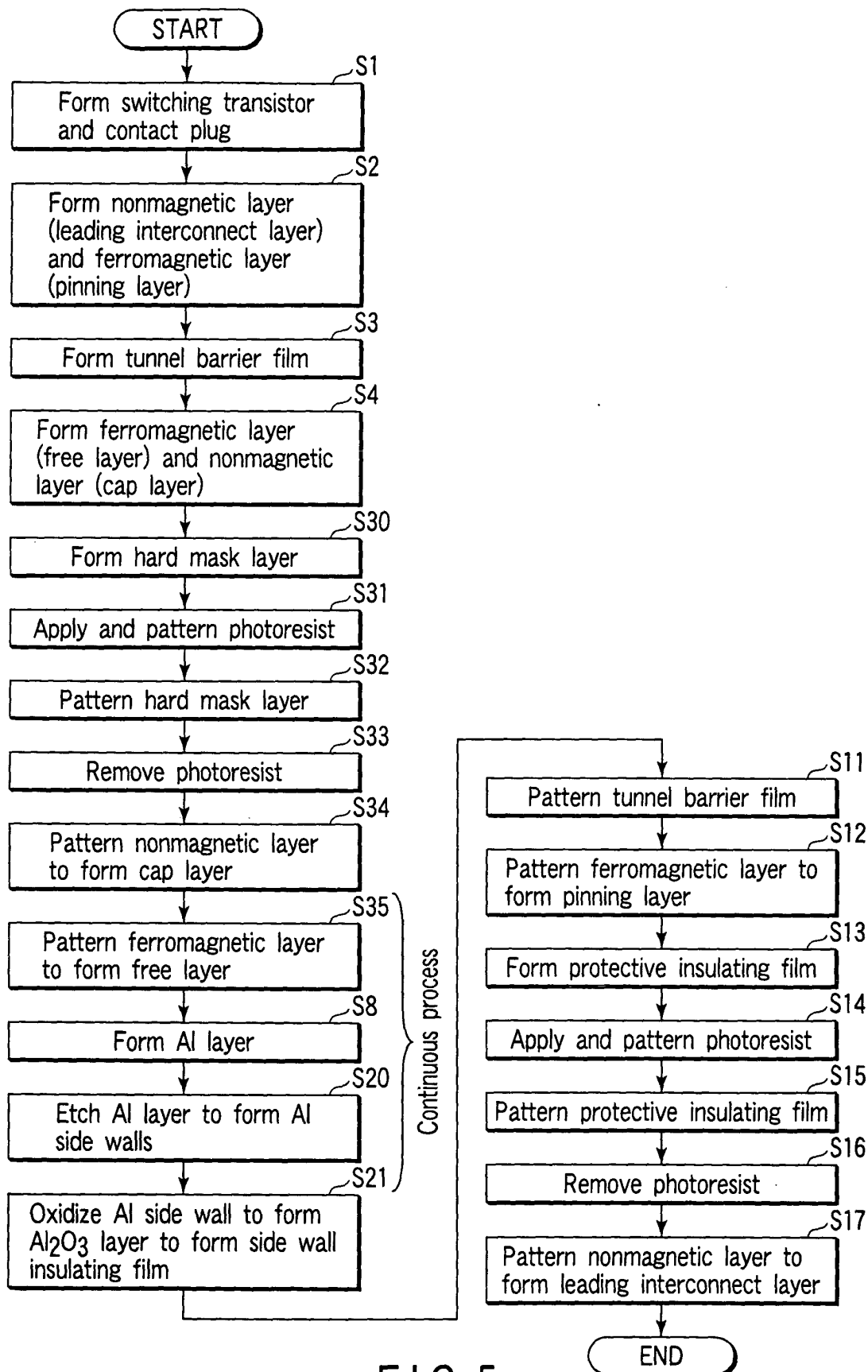


FIG. 5

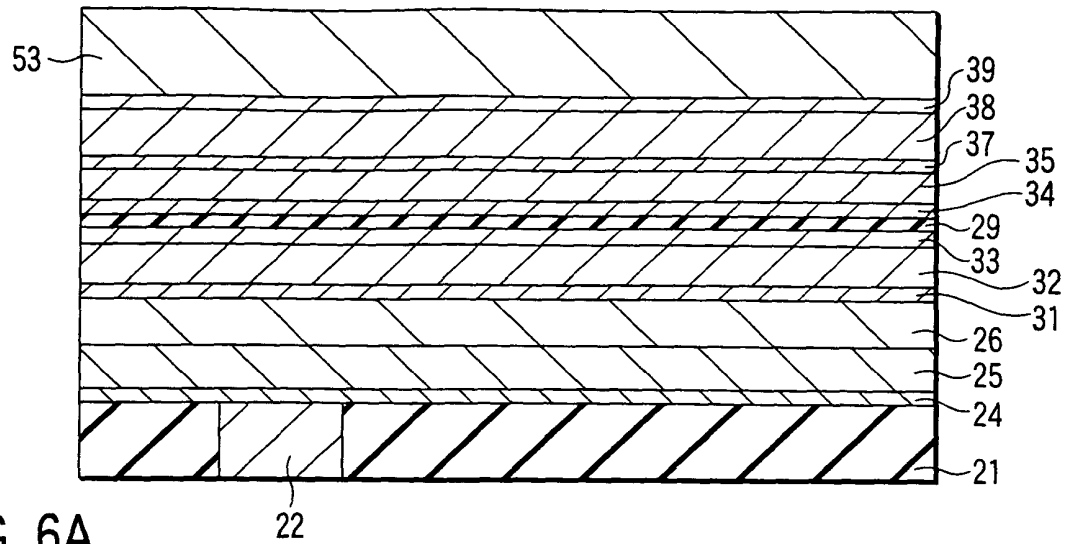


FIG. 6A

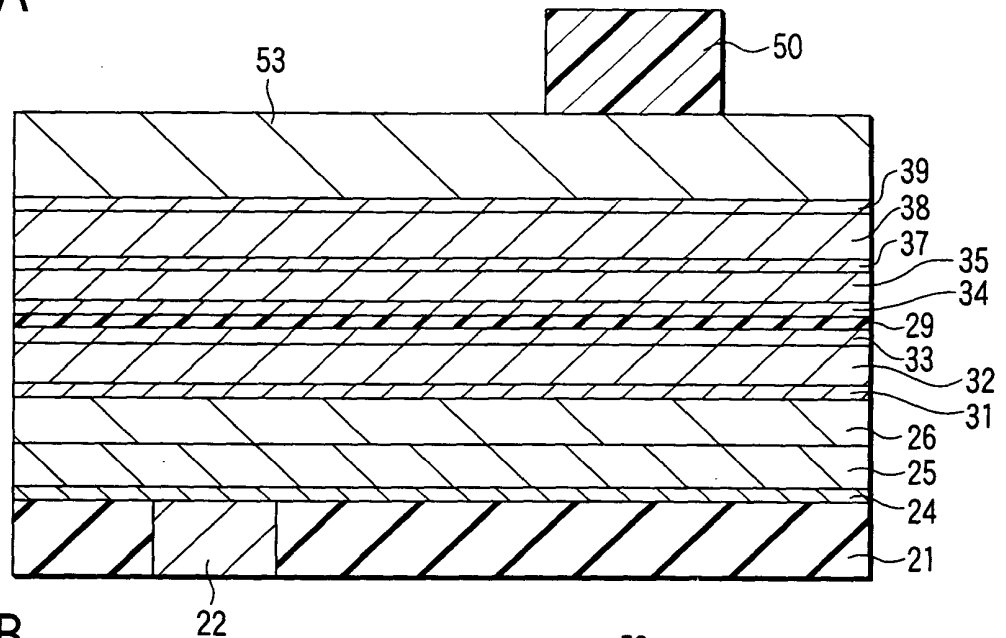


FIG. 6B

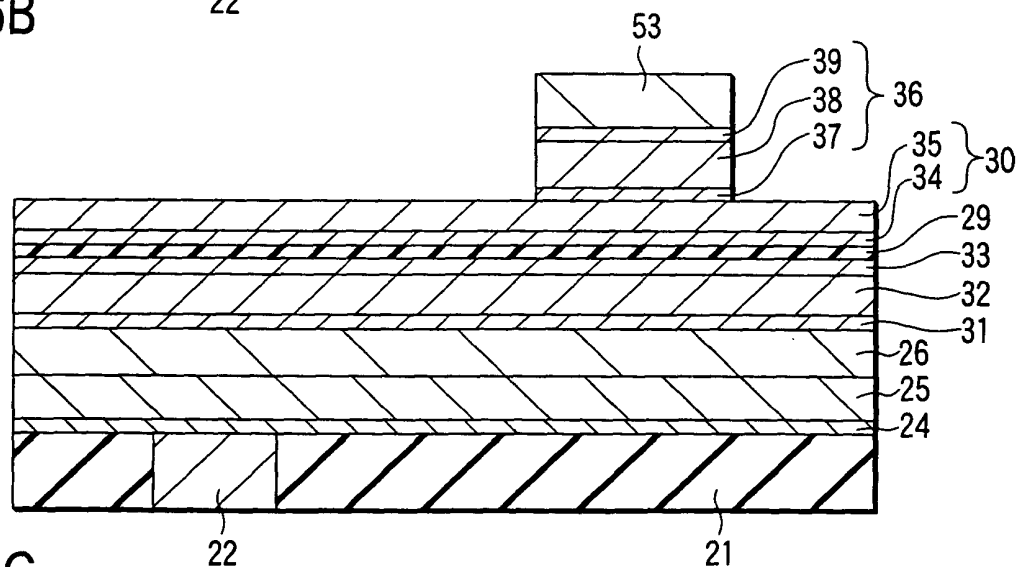
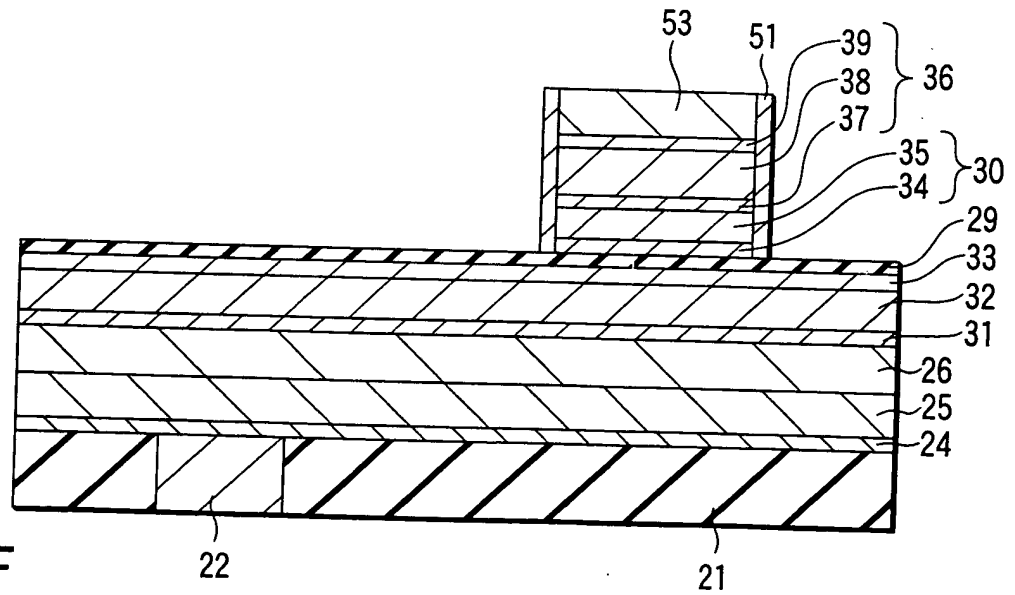
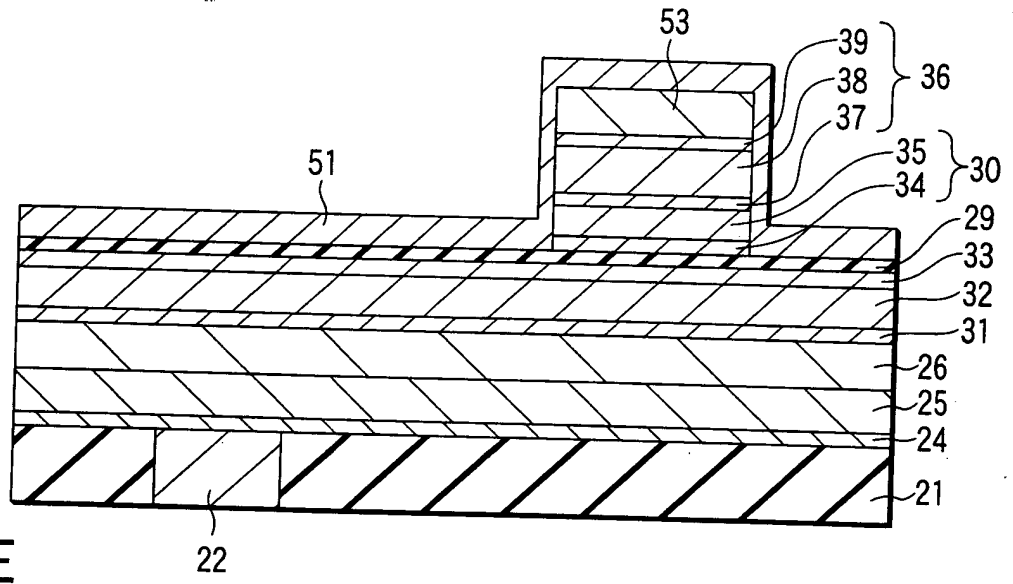
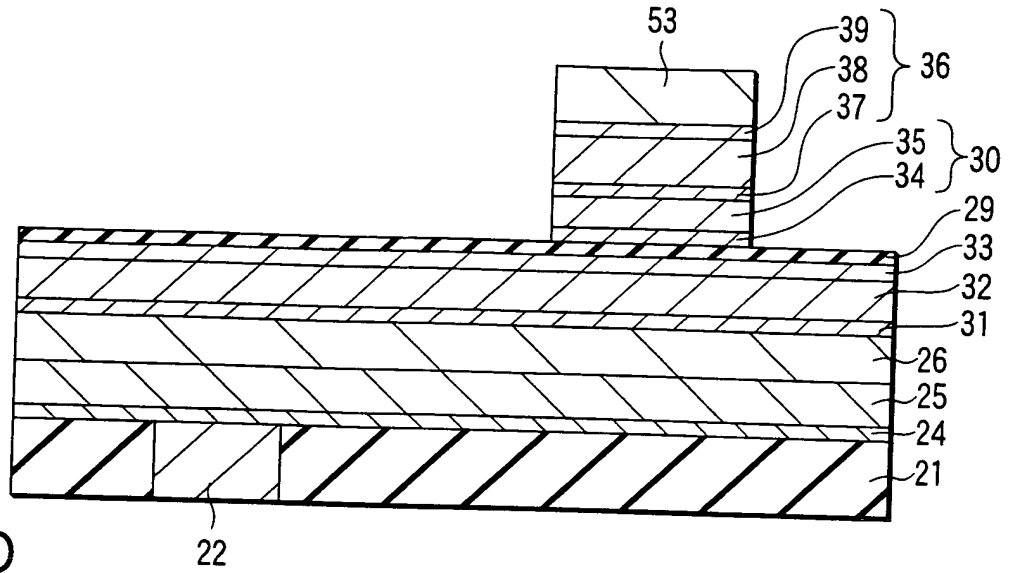


FIG. 6C



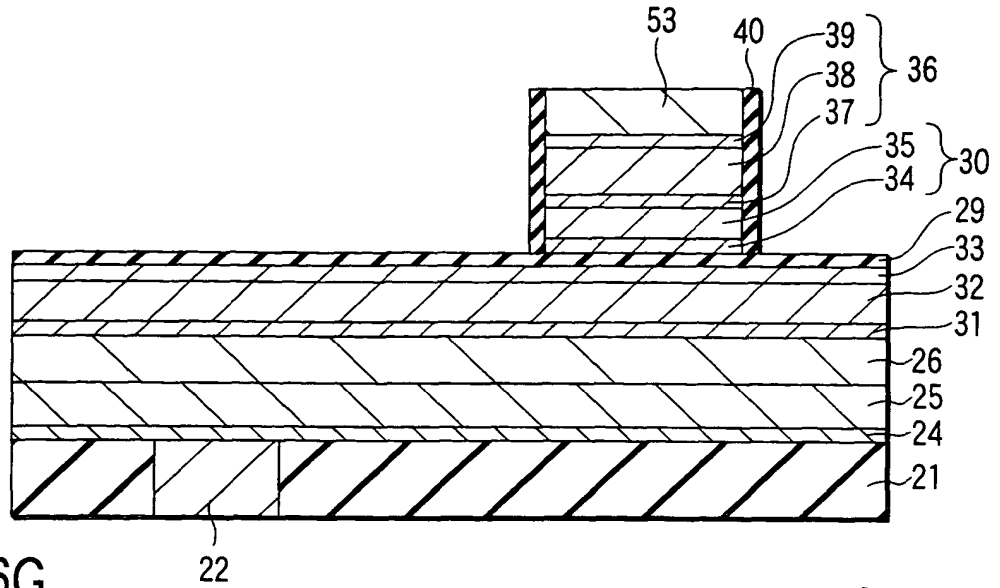


FIG. 6G

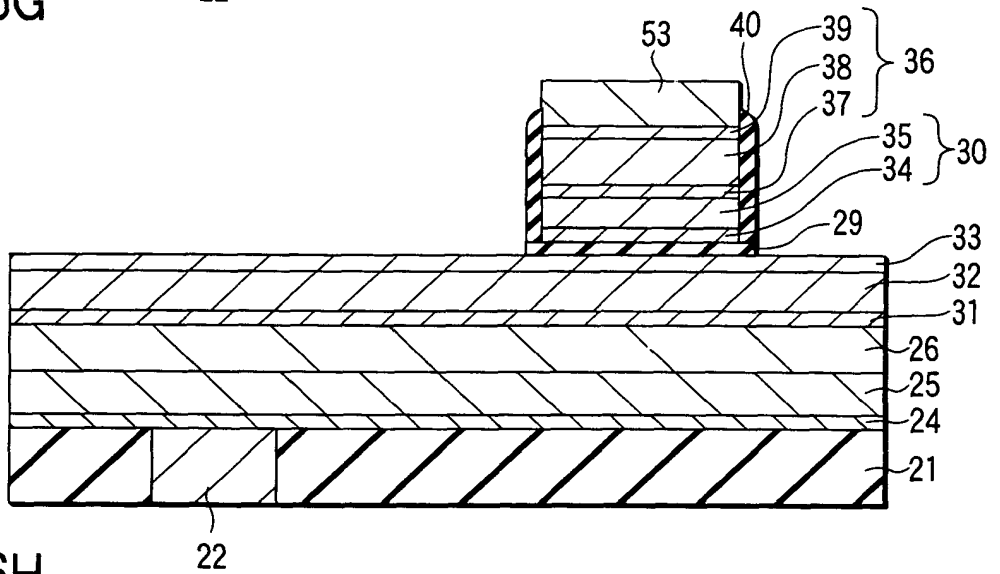


FIG. 6H

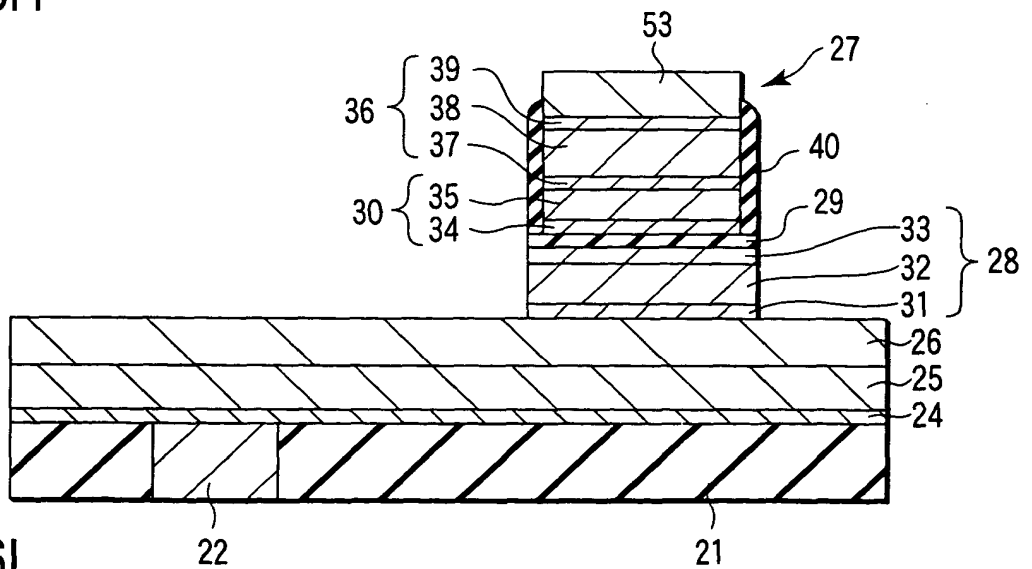


FIG. 6I

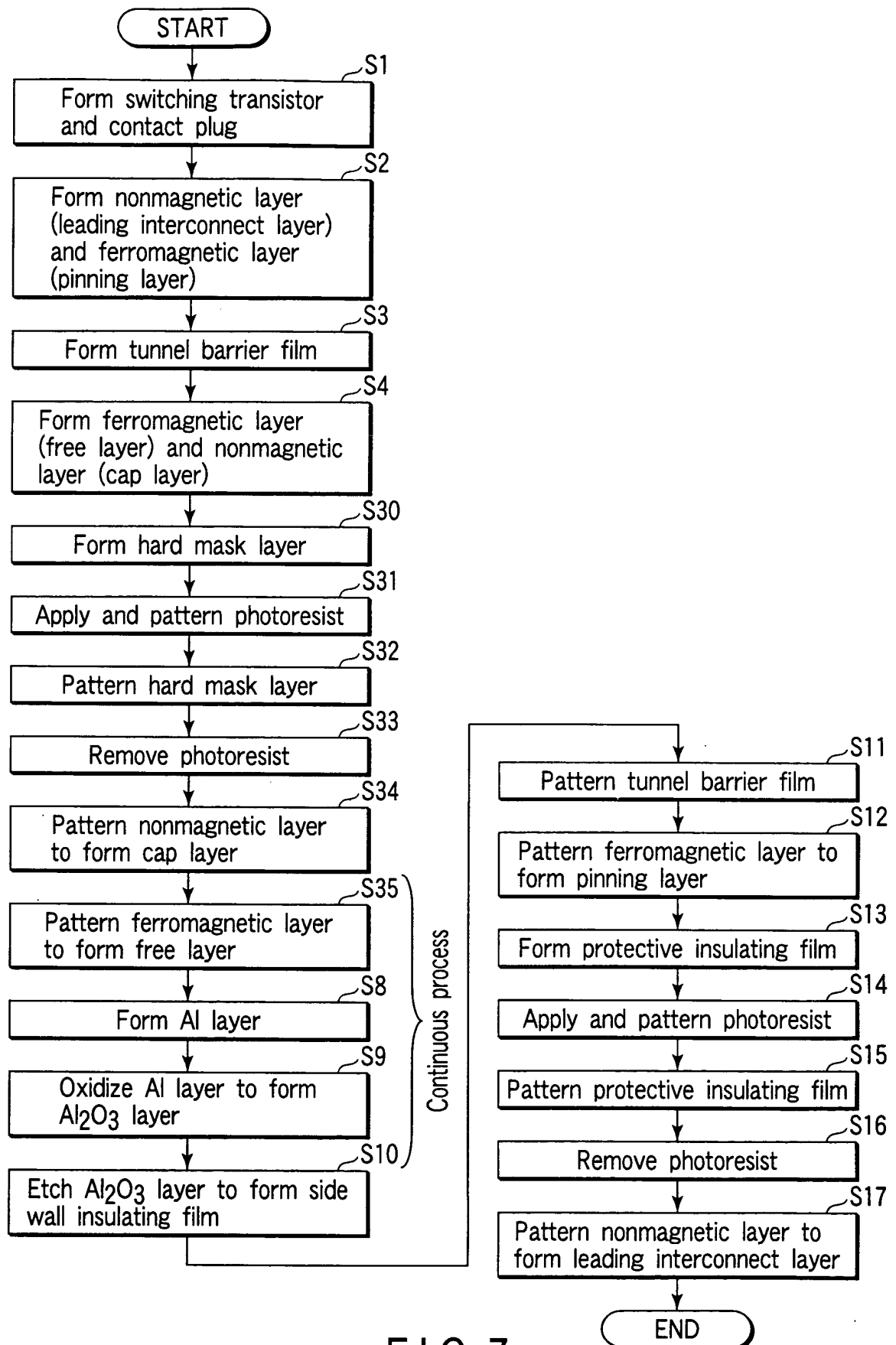
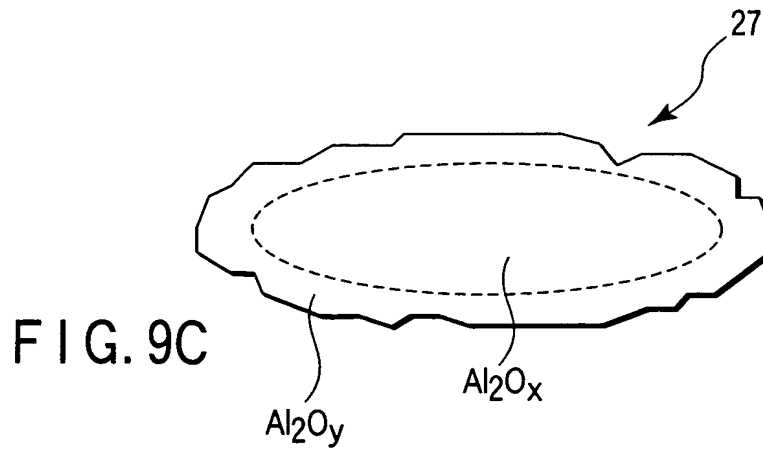
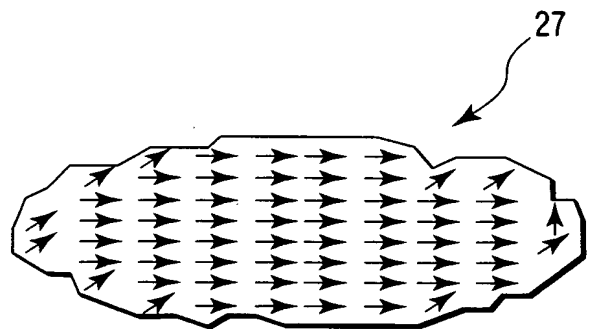
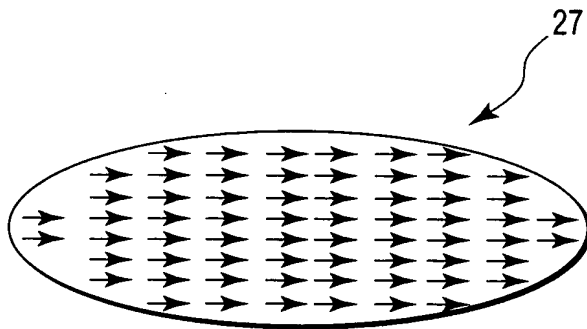
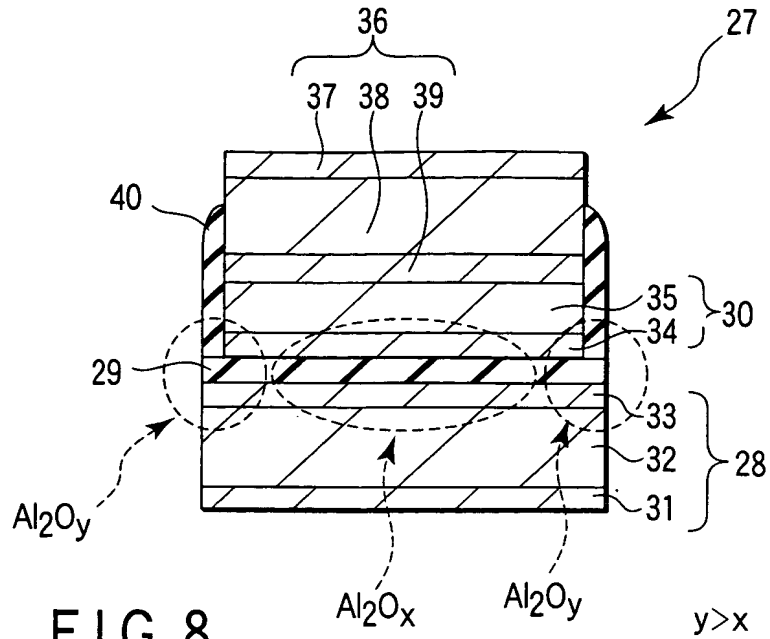
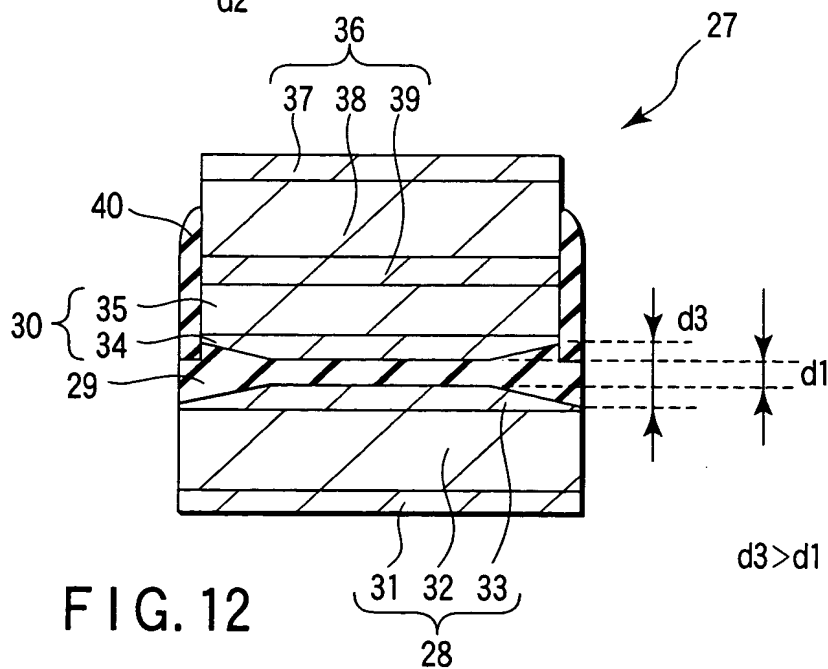
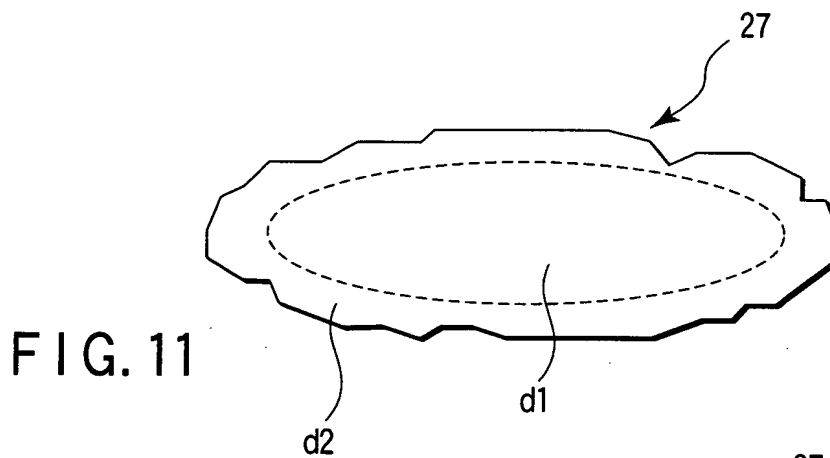
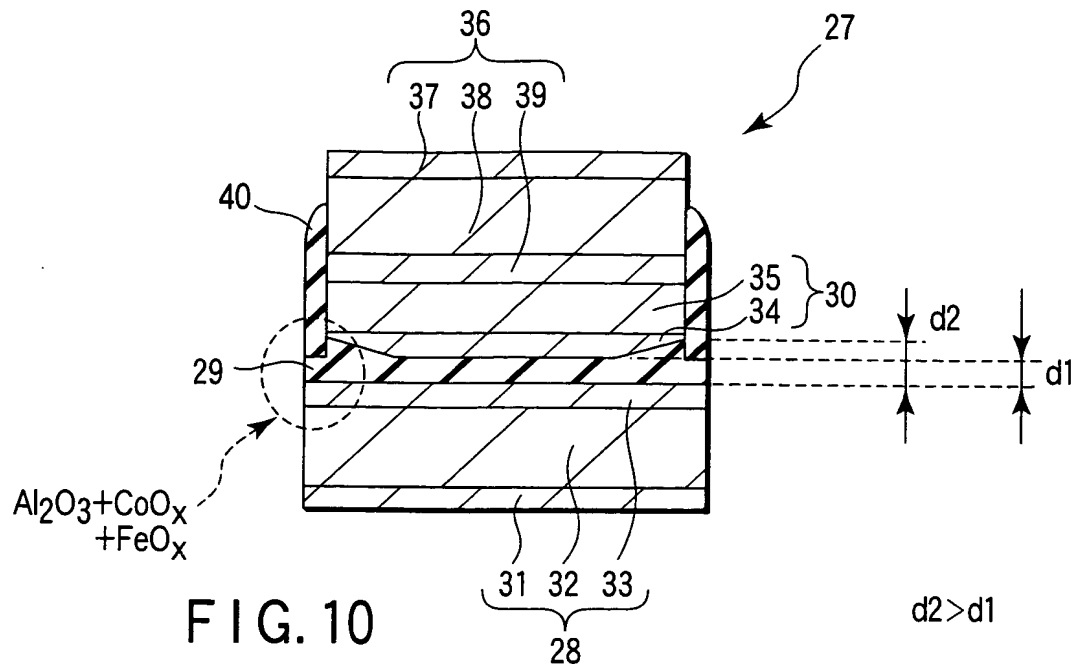
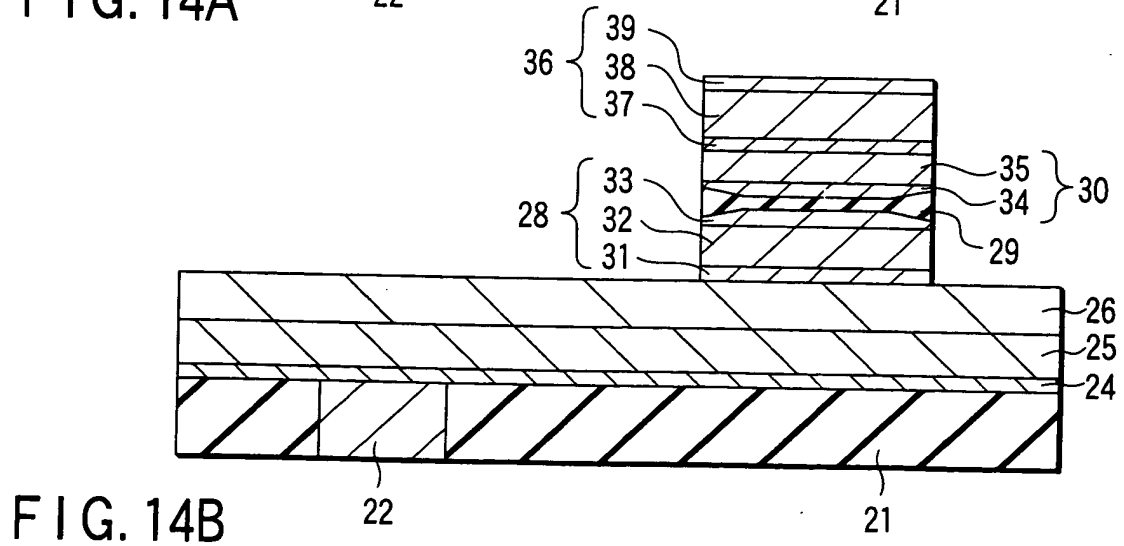
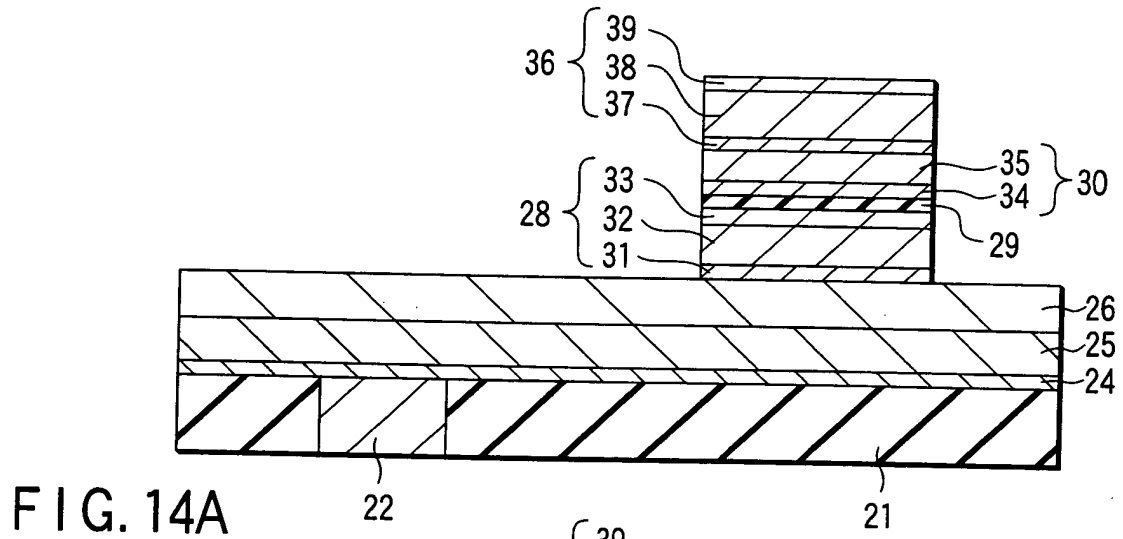
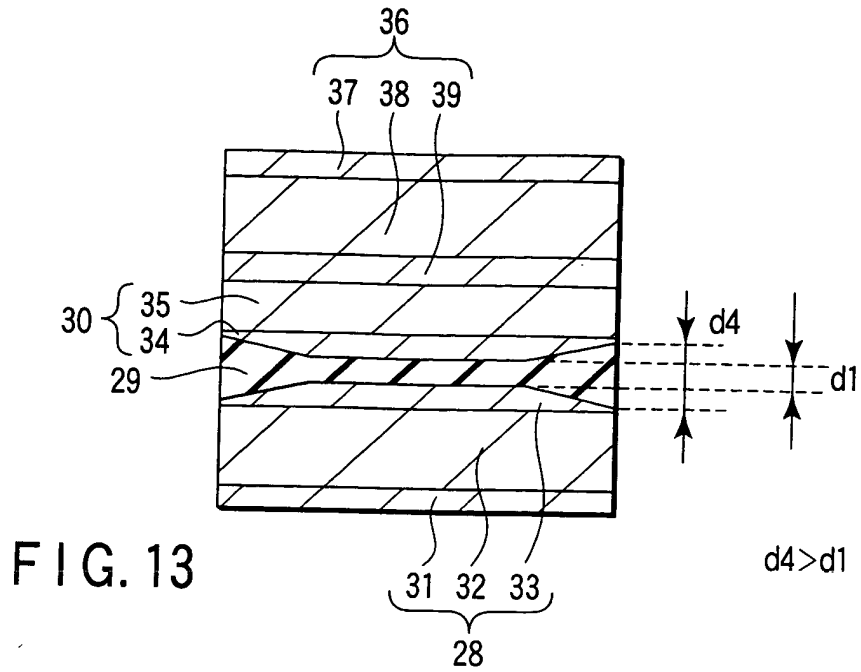


FIG. 7







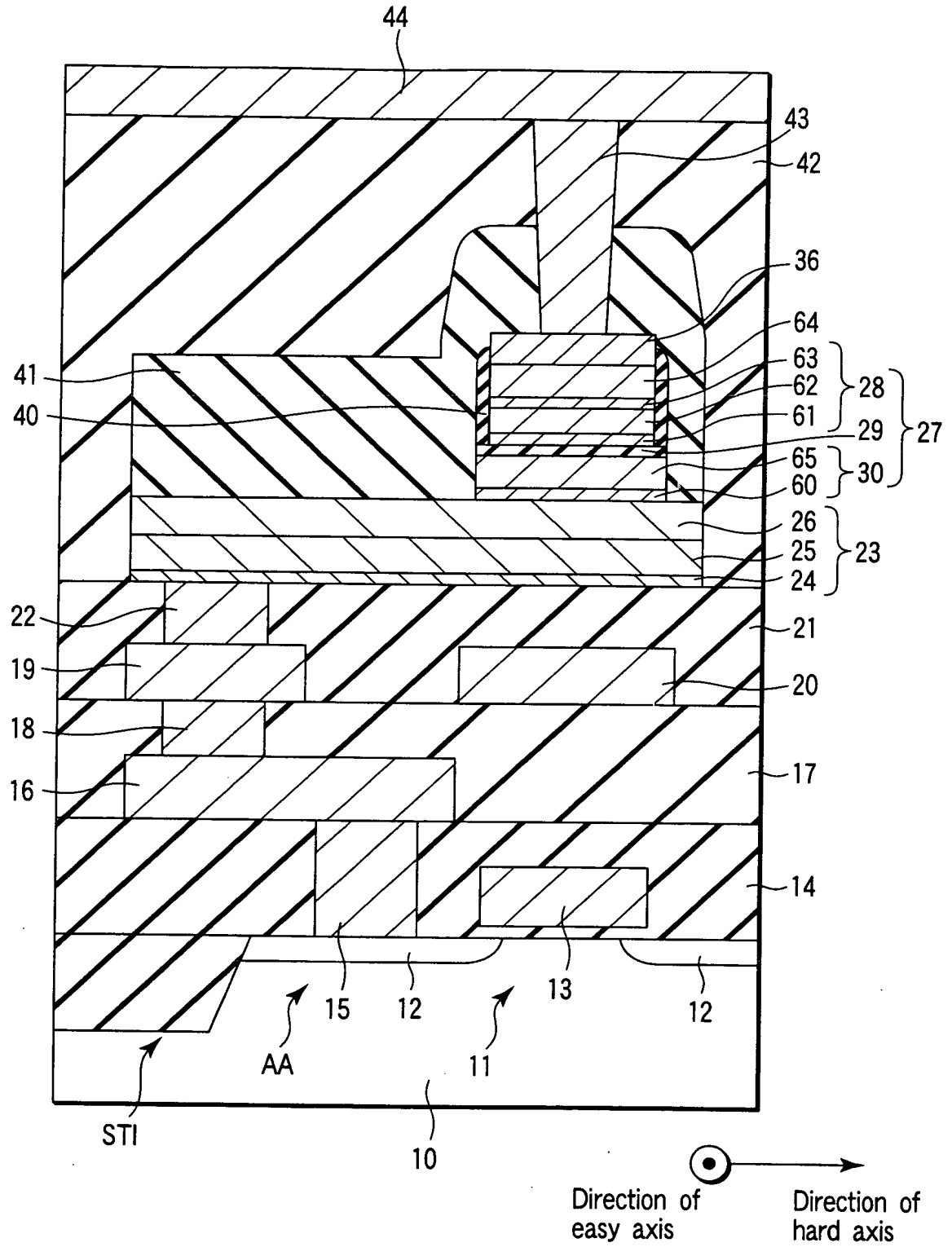
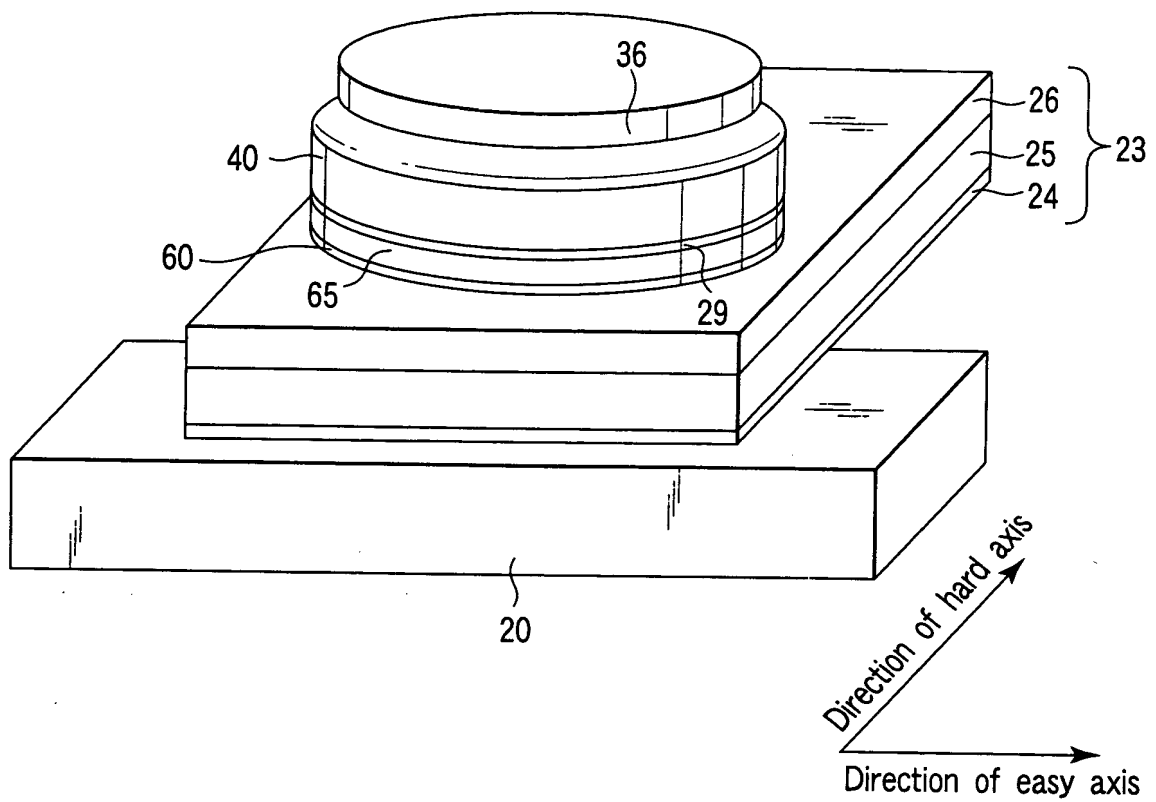


FIG. 15A



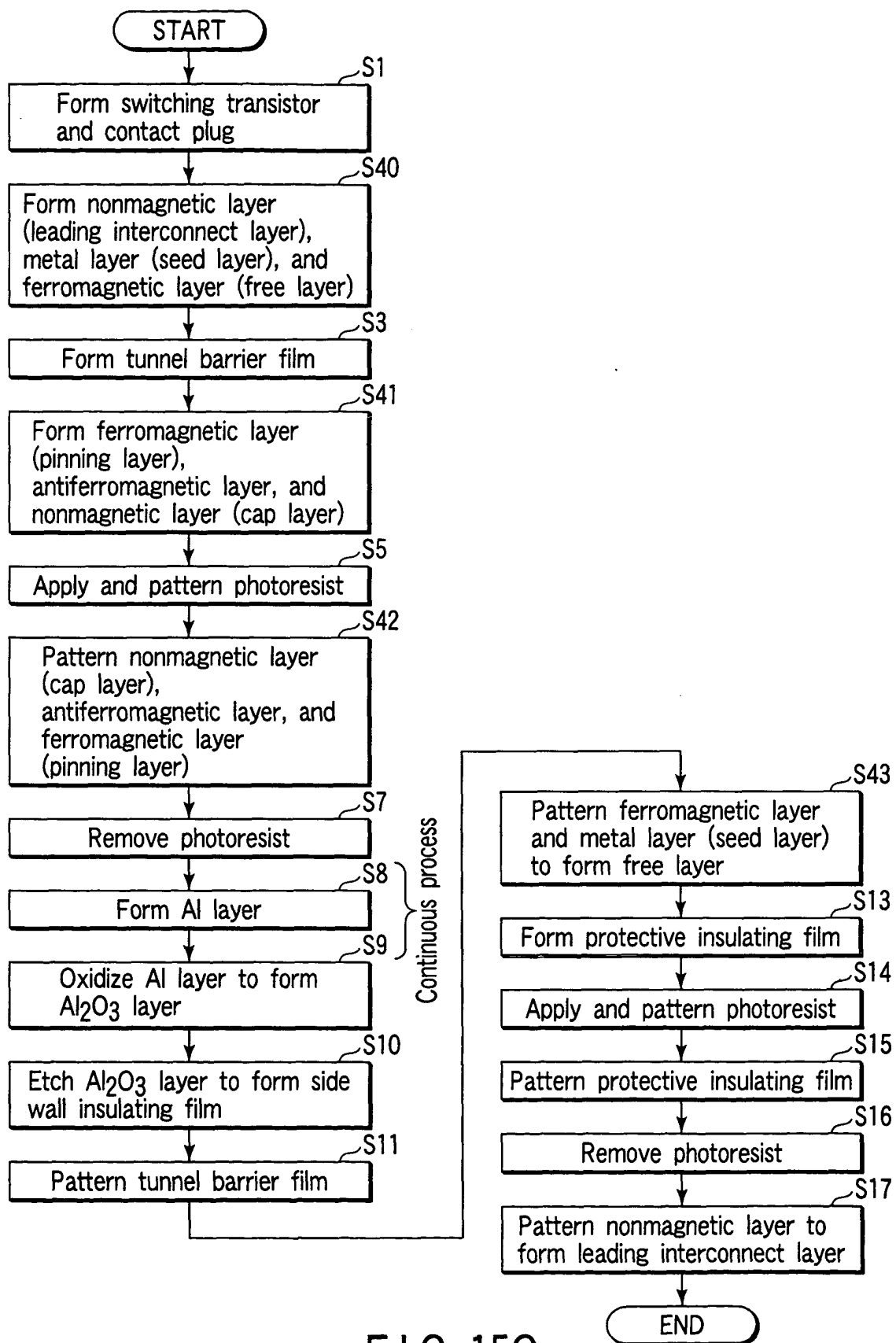
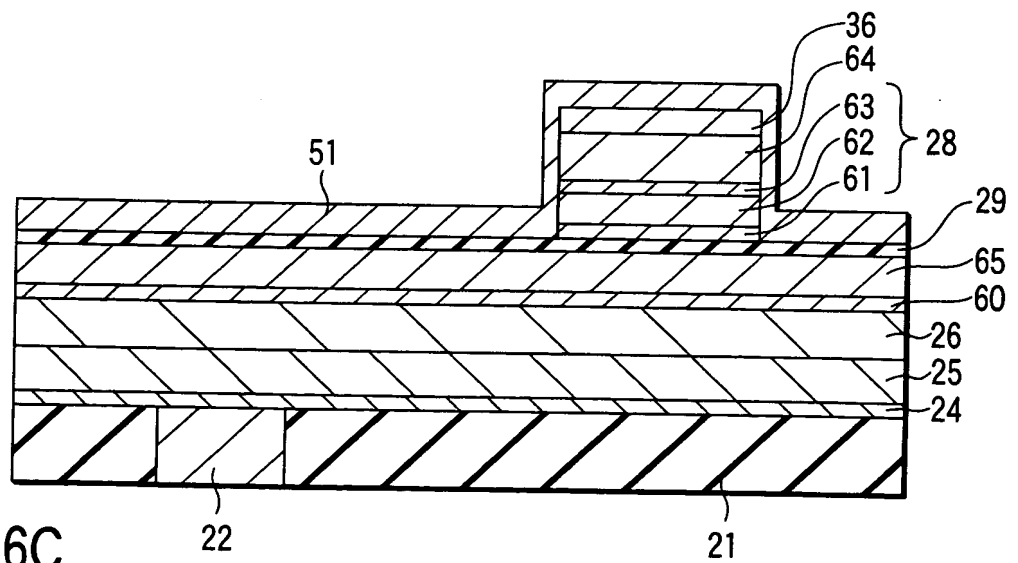
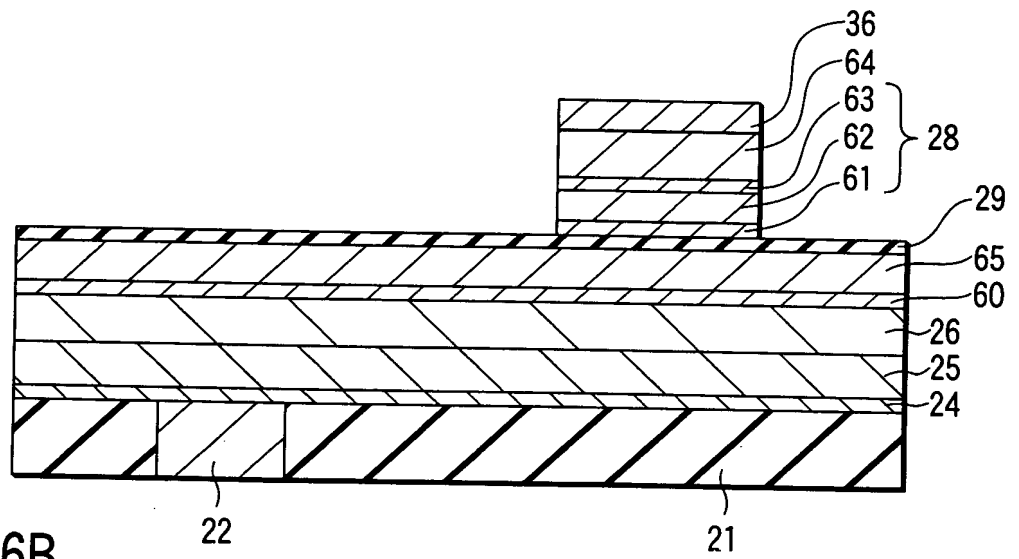
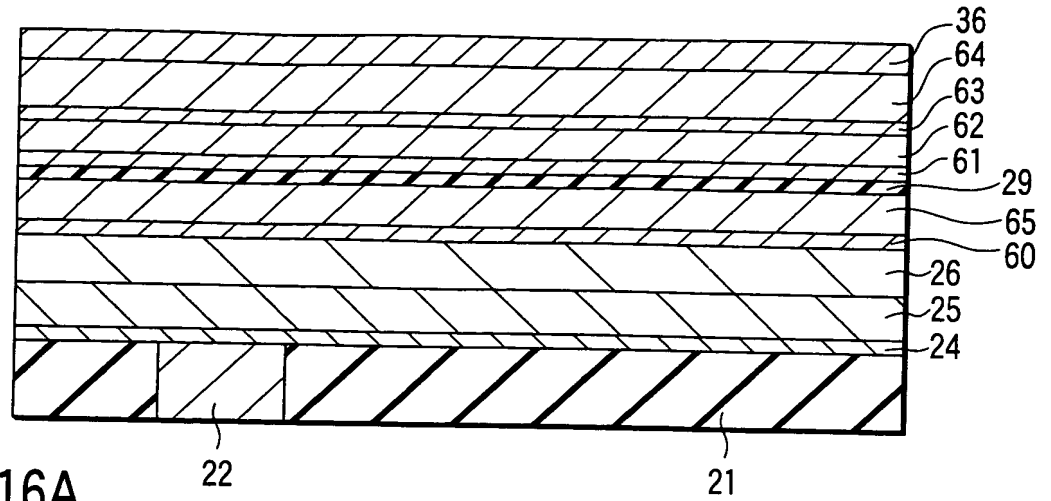
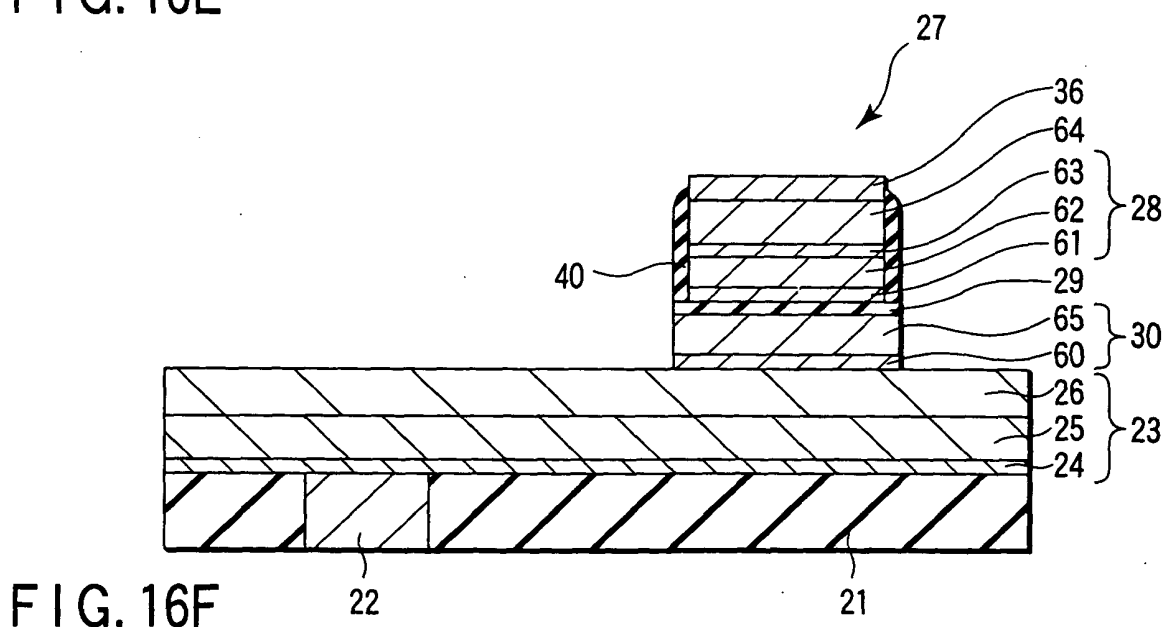
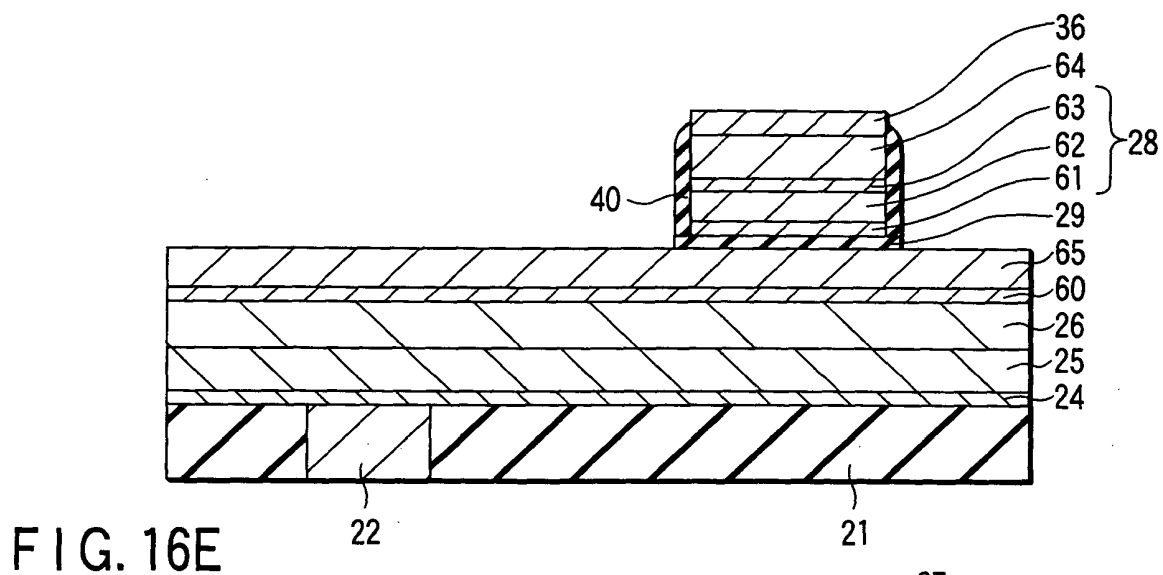
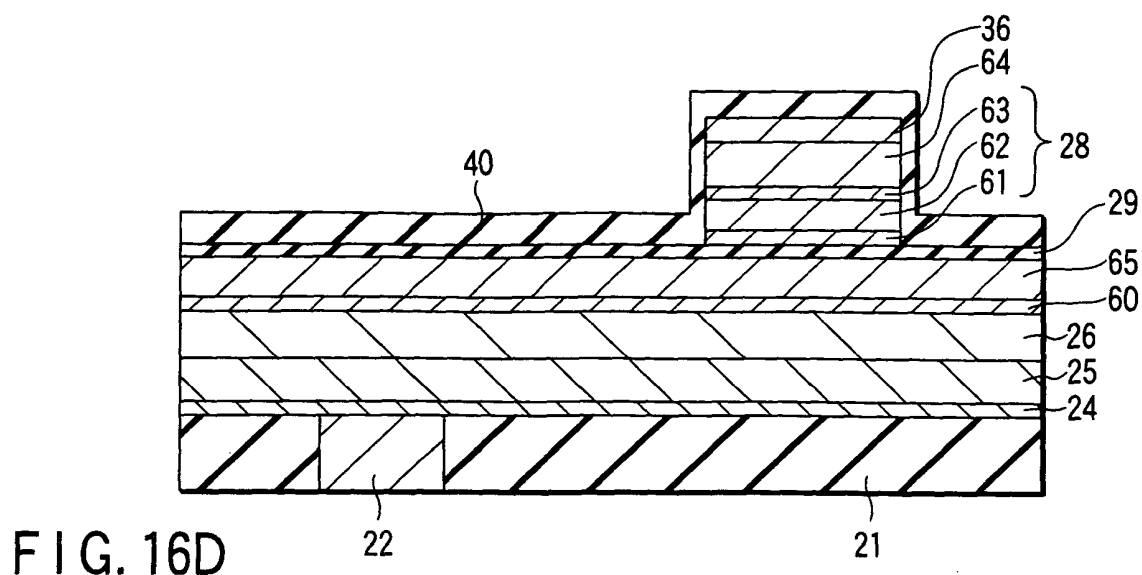


FIG. 15C





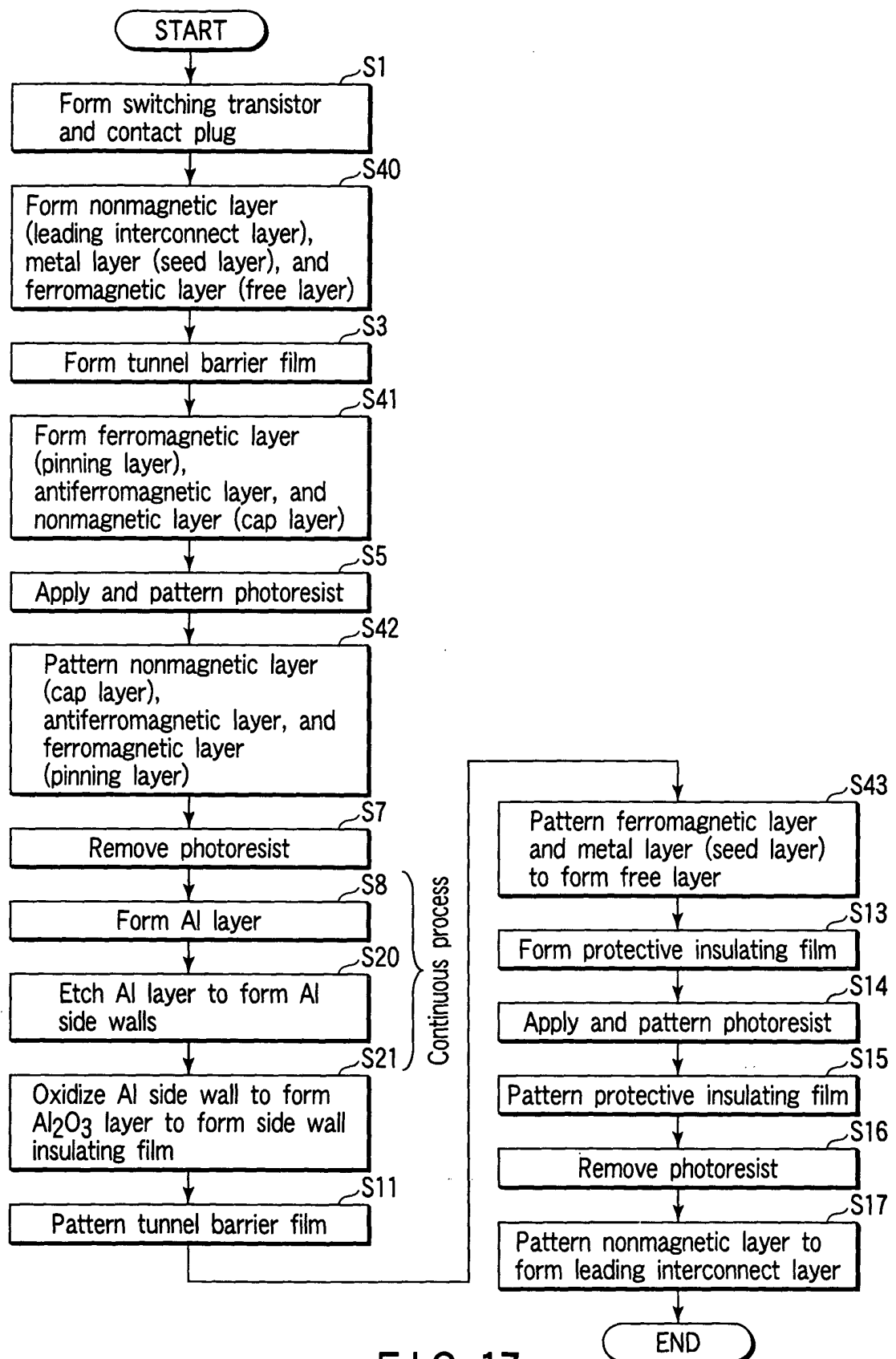


FIG. 17

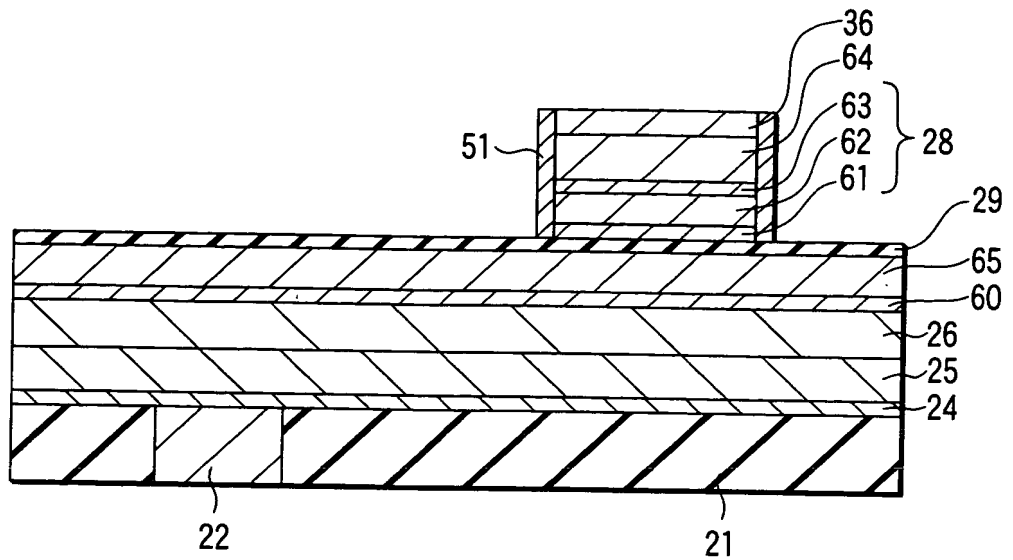


FIG. 18A

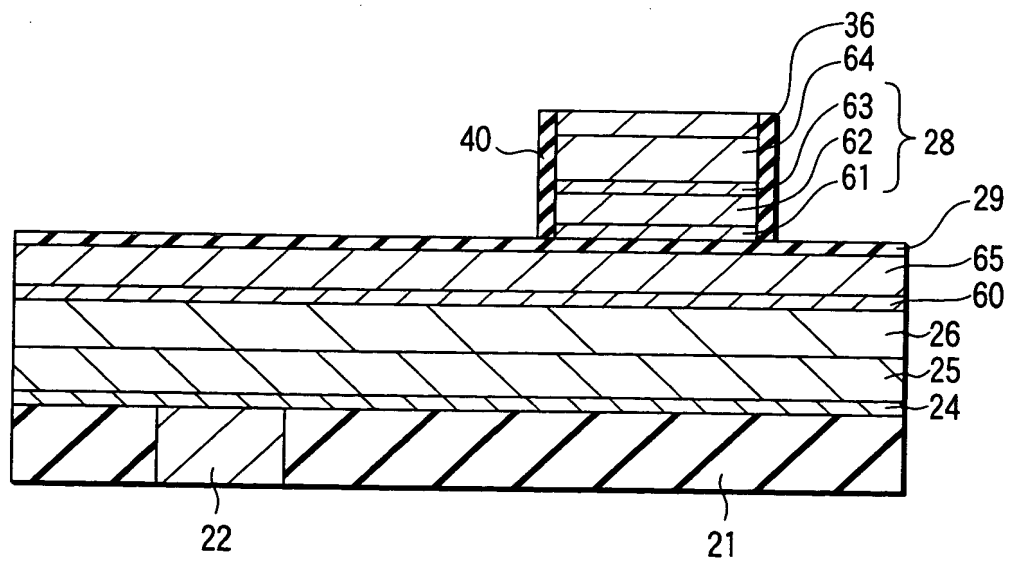


FIG. 18B

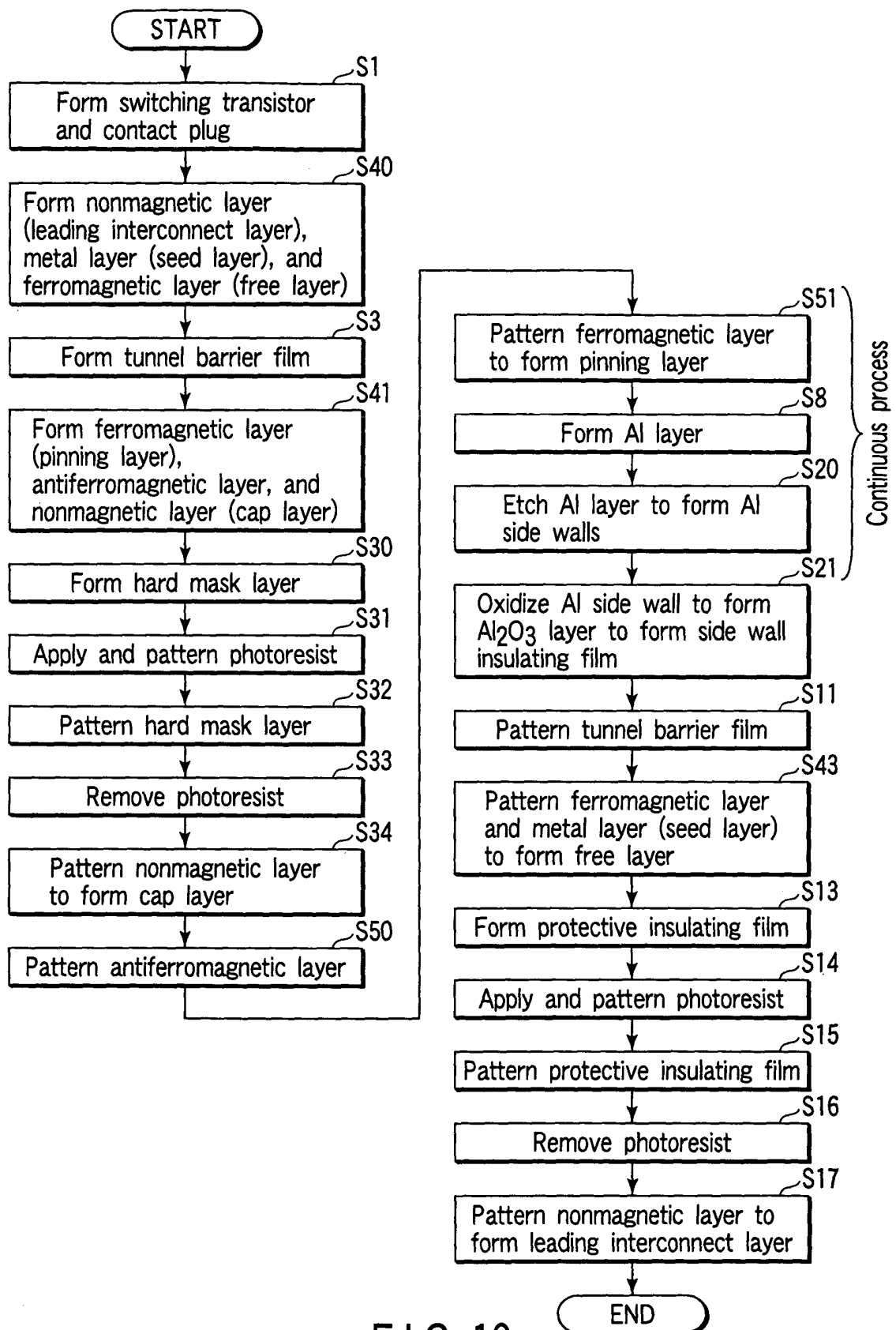
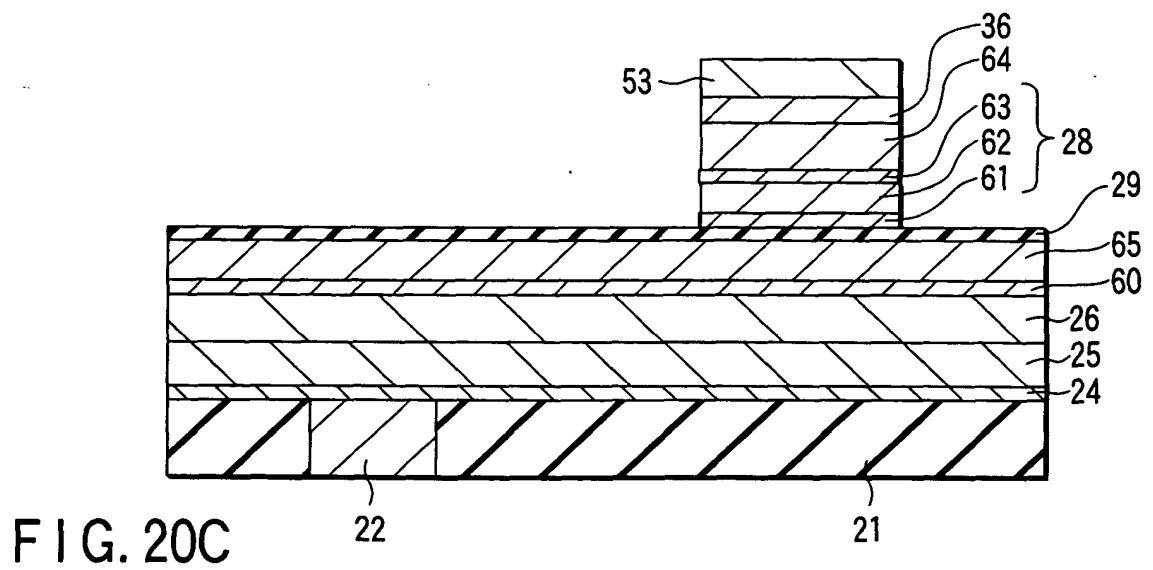
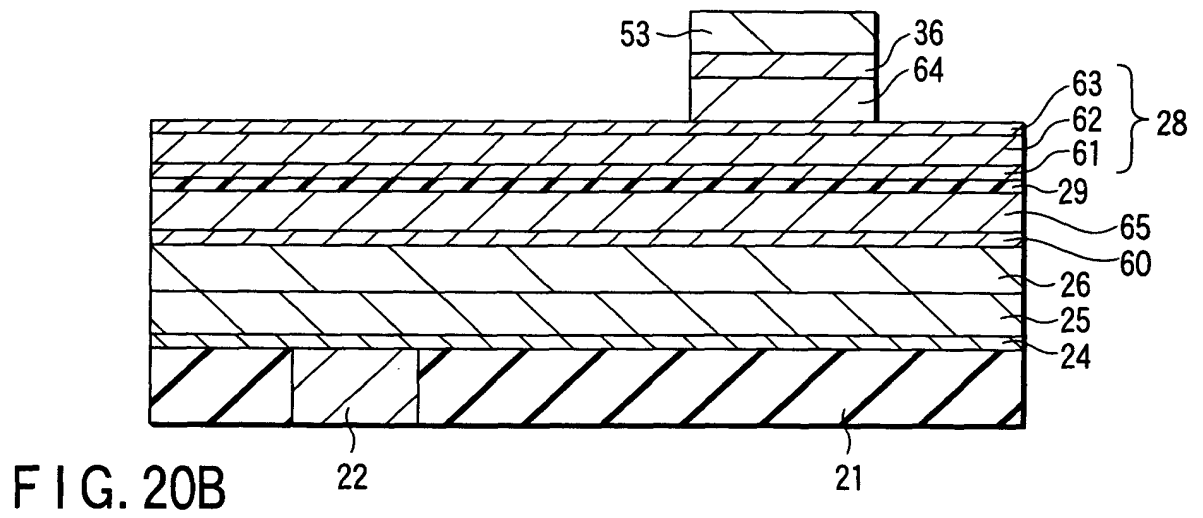
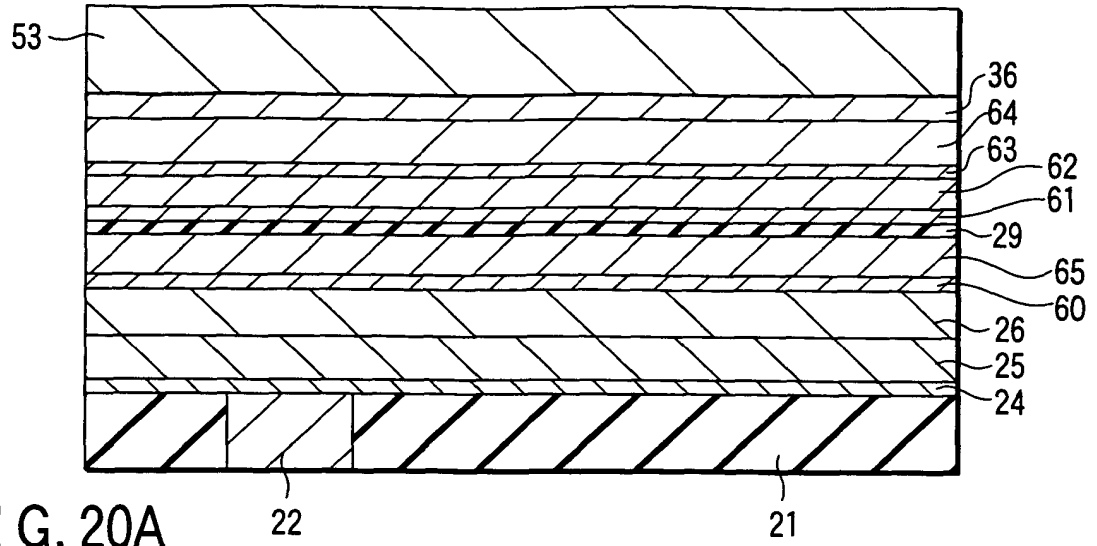
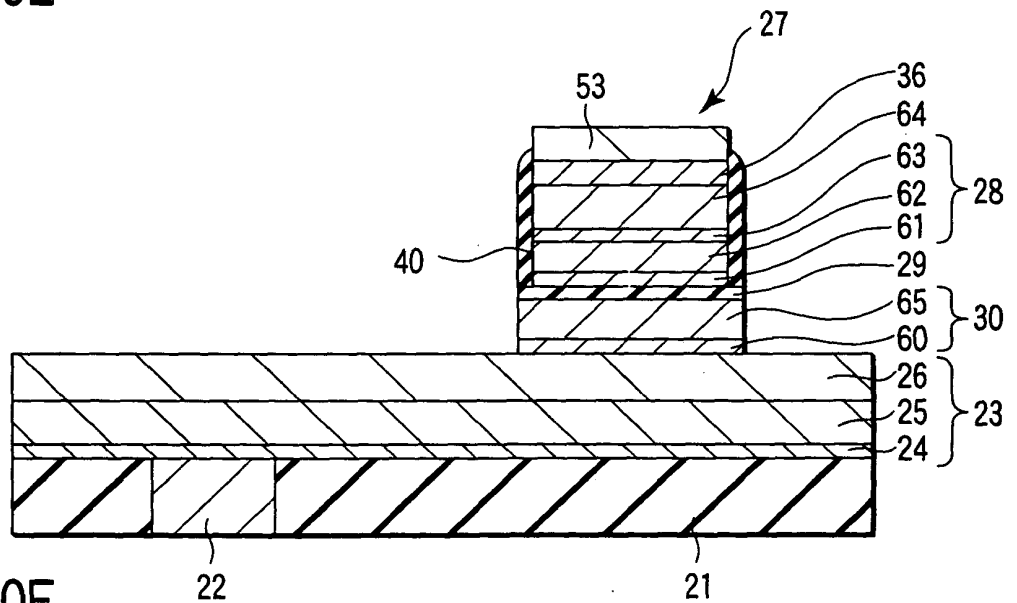
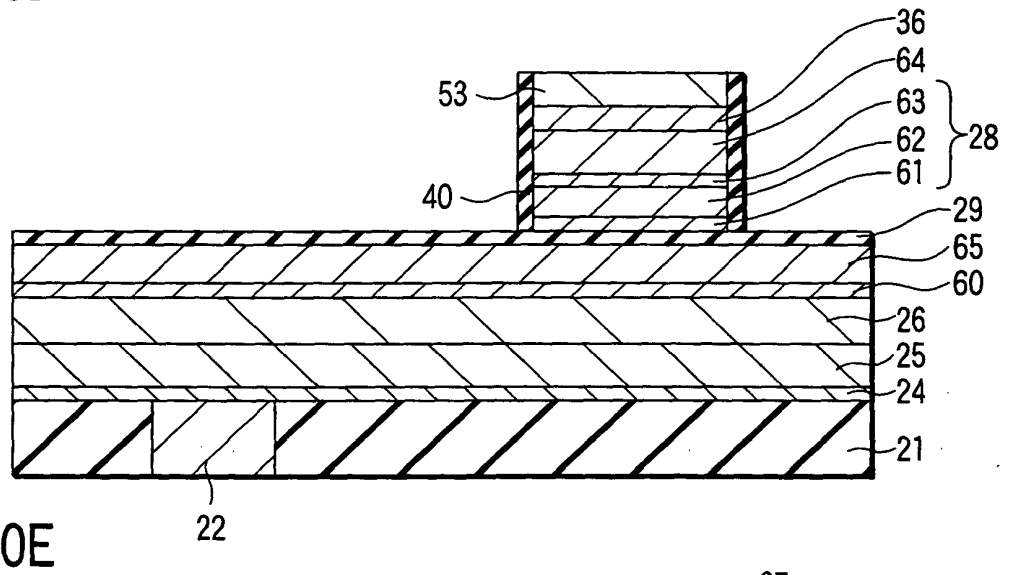
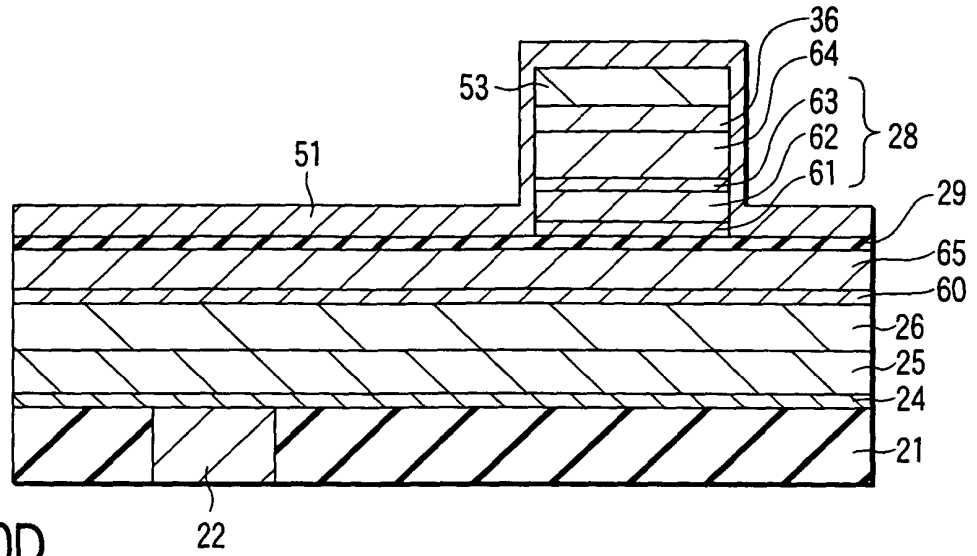


FIG. 19





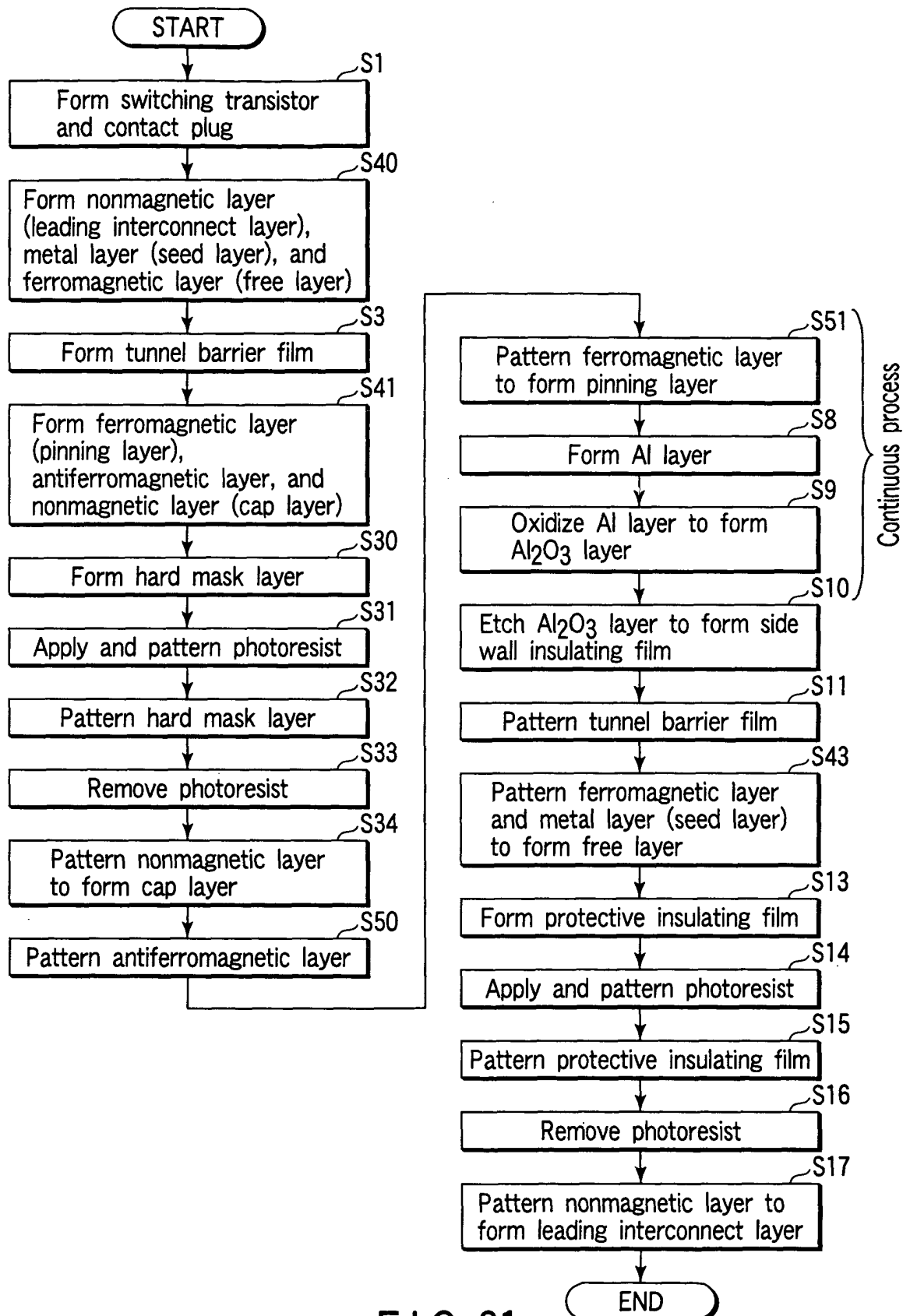


FIG. 21

FIG. 22

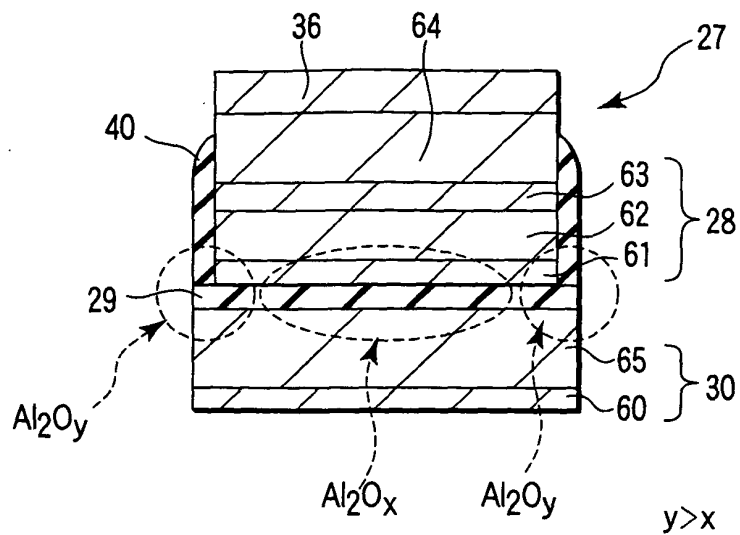


FIG. 23

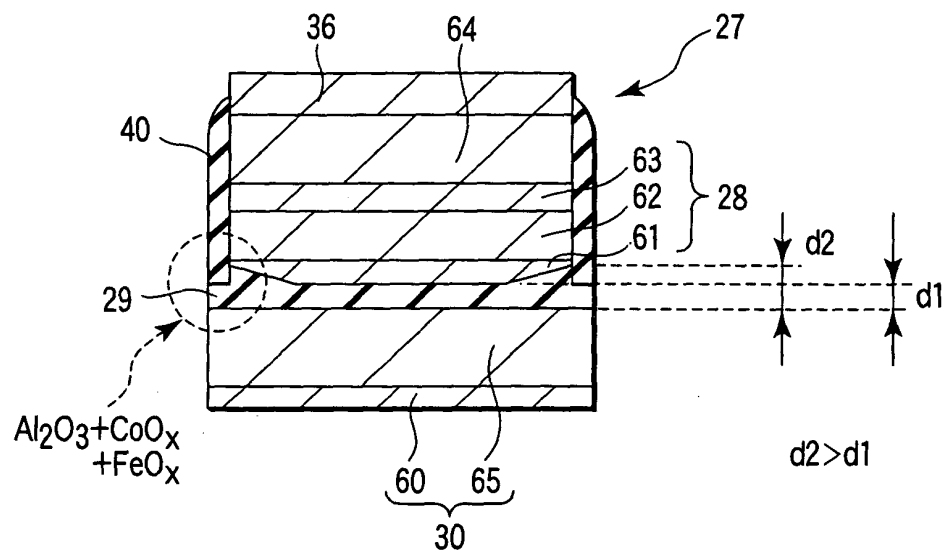
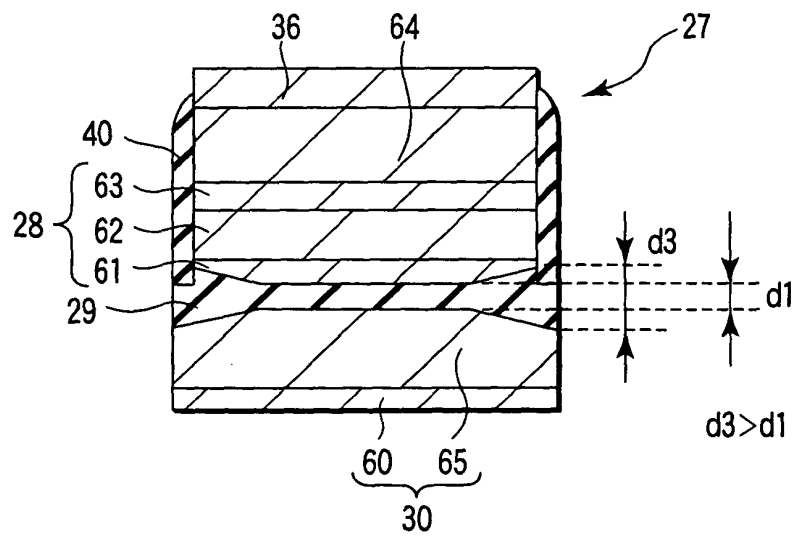


FIG. 24



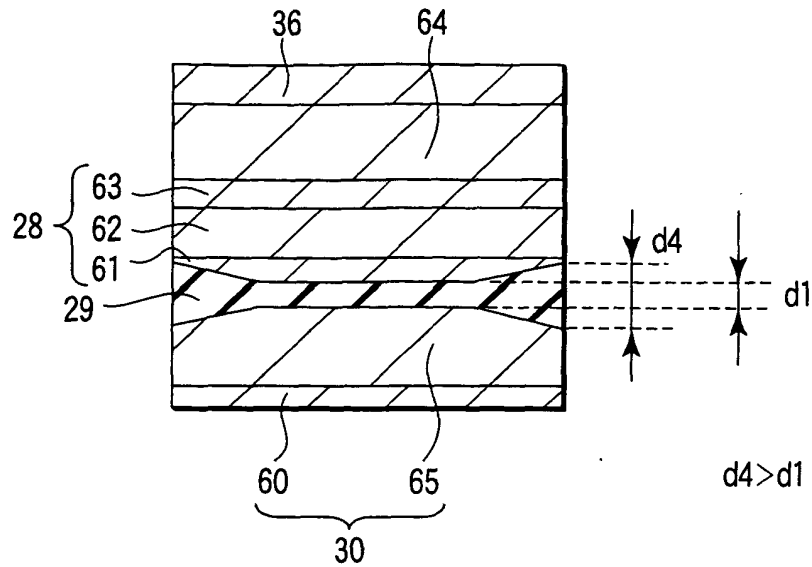


FIG. 25

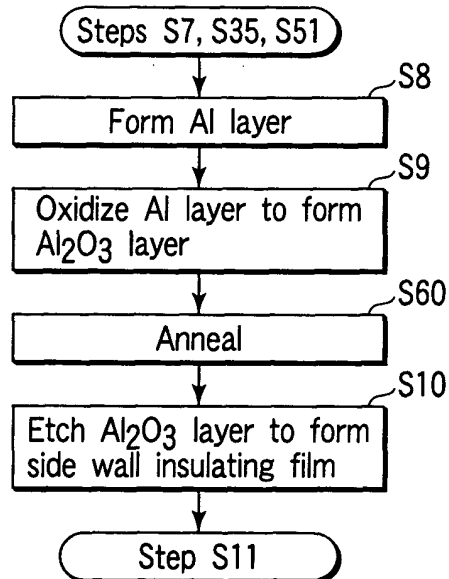


FIG. 26A

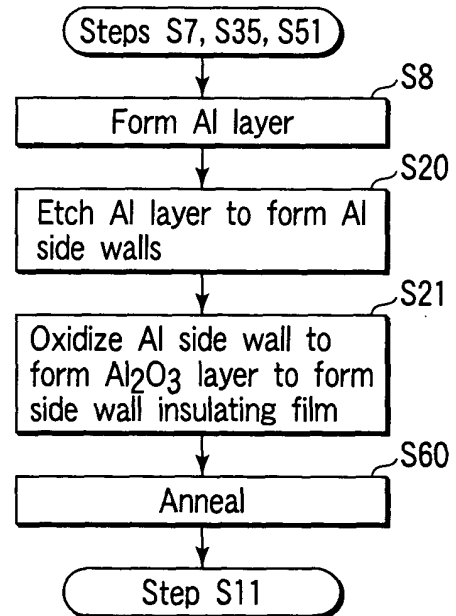


FIG. 26B

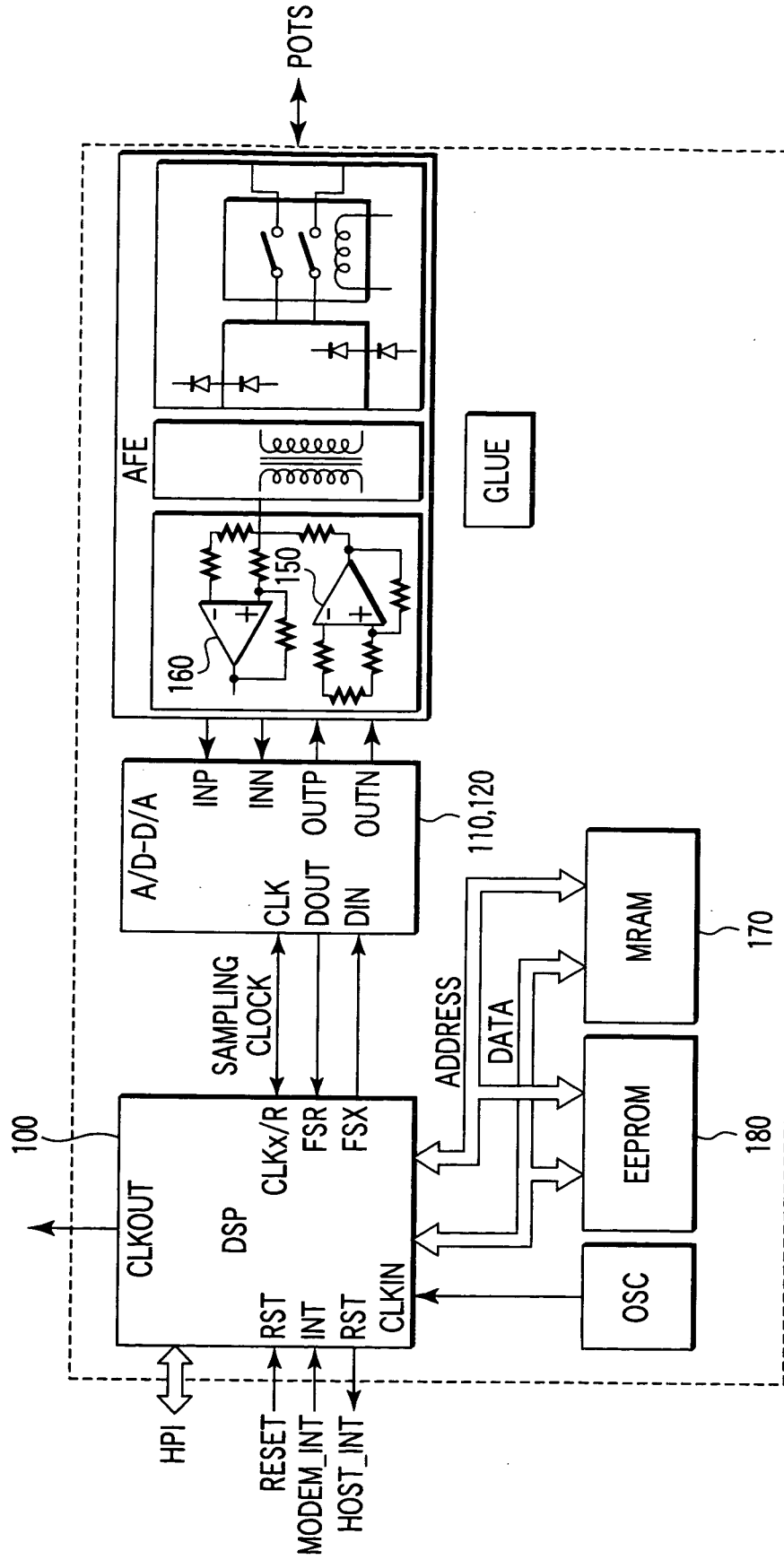


FIG. 27

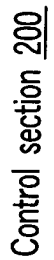
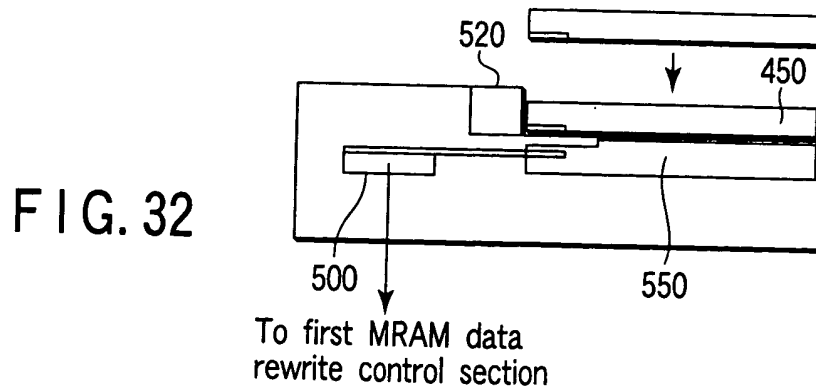
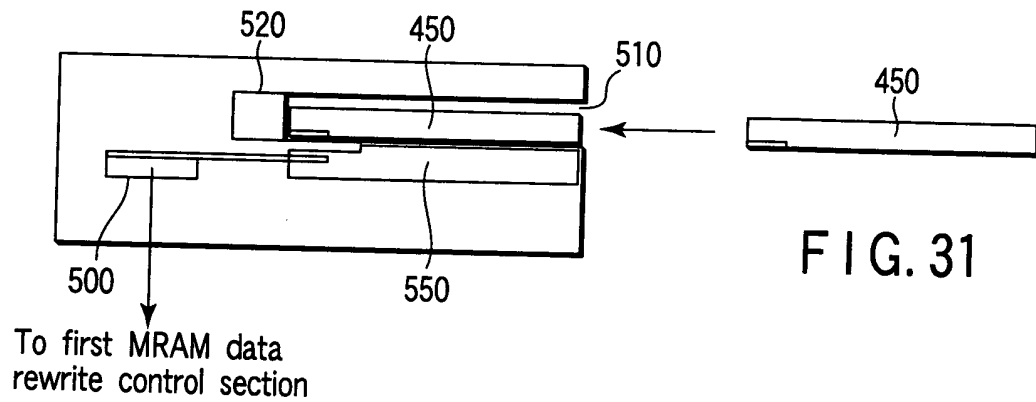
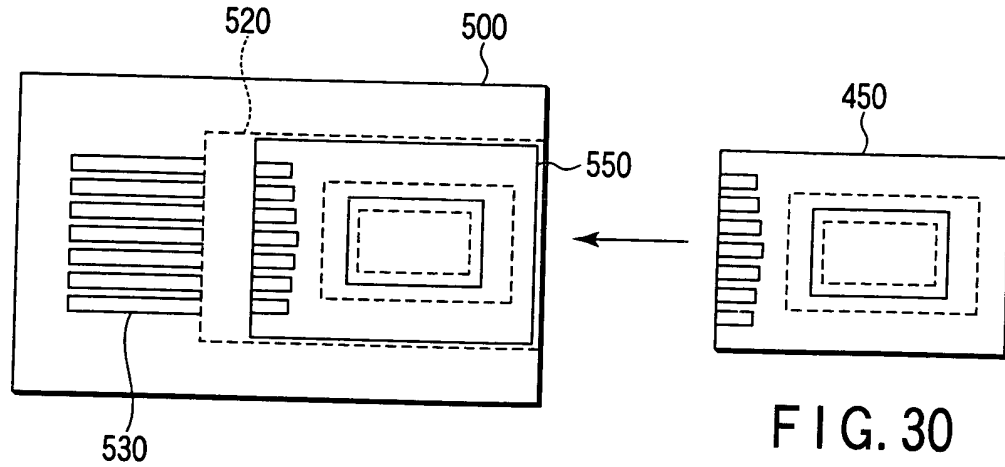
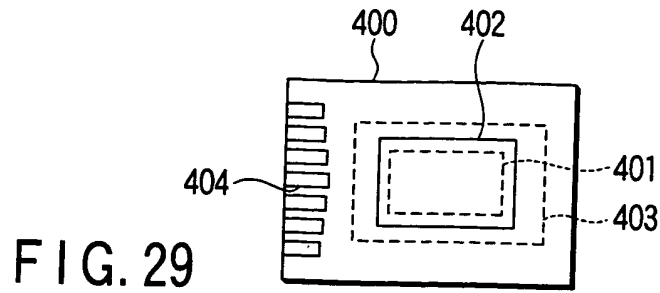


FIG. 28



To first MRAM data
rewrite control section

To first MRAM data
rewrite control section

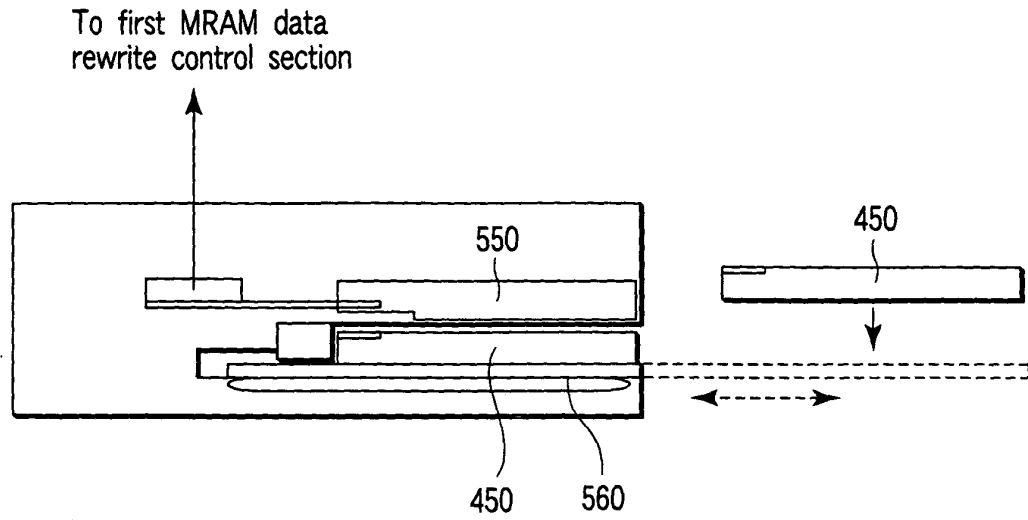


FIG. 33

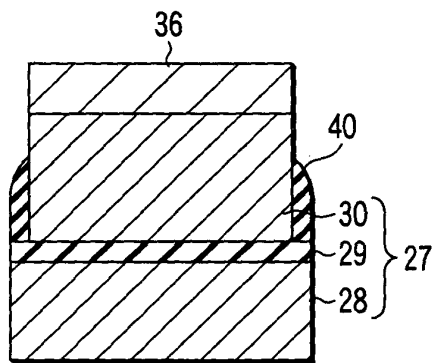


FIG. 34

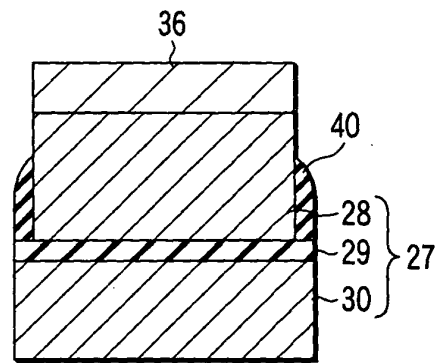


FIG. 35